Low-Power Architectures for Multi-Channel Intelligent Neural Interfaces

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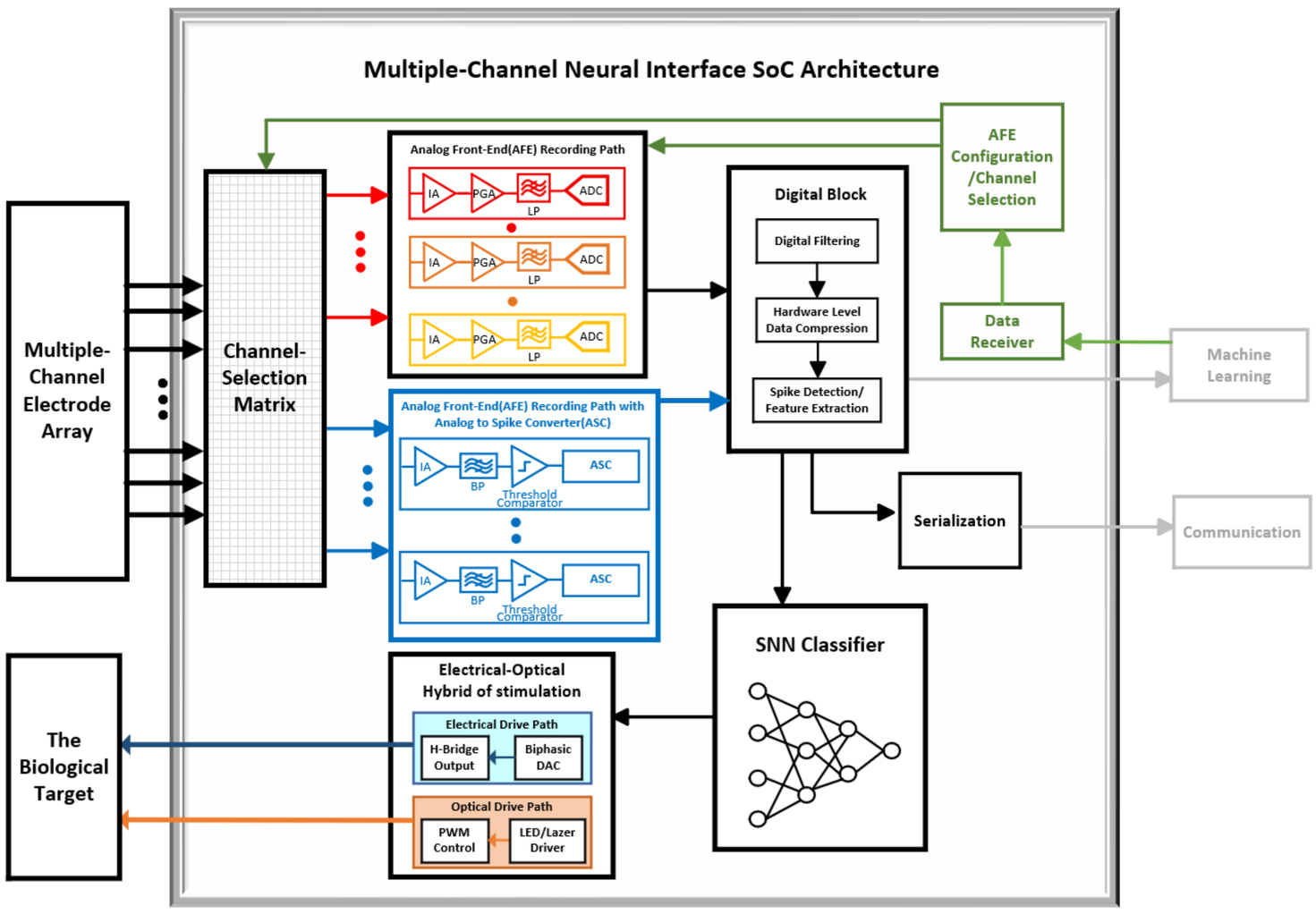
The title of this PhD Thesis is “Low-Power Architectures for Multi-Channel Intelligent Neural Interfaces”, which will focus on designing and optimizing the Neural Interface System-on-Chip(SoC). The aim of this project is to develop optimization solutions for Multi-Channel Neural Interface SoC which can achieve dynamically adapt system for power efficiency. The central technological requirement is a custom-designed optimization solution for power consumption and data transmission efficiency, with cleaning, processing and compressing data from spike signals acquisition.



Proposed Multiple-Channel Neural Interface SoC Architecture

Primary Objective

To design and optimize a low-power, intelligent multi(many)-channel Neural Interface SoC.

Secondary Objectives

- Develop intelligent on-chip optimization mechanisms that dynamically adapt system parameters—such as channel selection, bandwidth, gain, sampling rate, and data compression—in response to signal characteristics and application requirements.
- To design a loss-less solution for on-chip data compression and ready to be fed into a SNN or communicated depending on the need.
- To design a test platform for post-silicon evaluation of the SoC.

Background

The Brain-computer interfaces are neural prostheses that allow devices to communicate directly with parts of the brain.

Electrophysiological devices are extensively utilized to monitor neural activity across different scales, which range from measuring large-scale neuronal populations via electroencephalography (EEG) or local field potential (LFP) signals to record single-unit activity through intracortical electrodes.

Scaling the ensemble of recorded neurons and diversifying the targeted cortical regions will lead to substantial gains in BCI performance. As the number of recording channels effectively increasing, the volume of data required for transmission has also exponential growth. Furthermore, the overall power dissipation scales proportionally with the number of recording channels, presenting a significant challenge for high-density neural integration. As the complexity of neural decoding tasks grows, the SoC must operate under stringent power constraints to support multi-channel front-end integration

Methods

This project will design in system level, which is to optimize different chips already developed or under development in the group to be used for multiple or many channels, including diverse path for example:

- To explore a solution to sort and reconfigure Analog-Front-End (AFE) channels based on important scores (depending on the target specs) of each channel which are assessed by machine learning or other algorithms.
- Specific filtering circuits will be designed to clean and data targeting on-chip neural signal data compression and decoding.
- To design a loss-less neural signal data on-chip compression scheme by taking advantage of spatial correlation and temporal correlation between adjacent channels.
- To use neuromorphic or similar processing models for a fast and energy-efficient decision making for optimization of the SoC.
- Post-layout verification will be followed by tape-out and evaluation via a custom-designed test platform. The finalized SoC will then be integrated into a real-time computing system for cross-scenario performance validation.