

Neuromorphic Bioelectronics for Brain-Computer Interfaces: CMOS Design of Analog Front-End and Sensor Interfaces for Wearable Neuroprosthetics

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The project Neuromorphic Bioelectronics for Brain-Computer Interfaces: CMOS Design of Analog Front-End and Sensor Interfaces for Wearable Neuroprosthetics is part of the NeuroMate project which aims to develop a next-generation assistive glove controlled through electroencephalography(EEG) potentially merged with other biosignals if necessary, enabling stroke patients to perform functional movement rehabilitation at home. A central technological requirement within NeuroMate is a custom-designed analog front-end (AFE) optimized for EEG signal acquisition through wearable EEG electrodes, with constraints on power consumption, size, noise performance, and long-term stability.

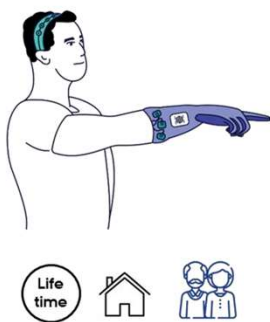


Figure.1 EEG headset and assistive glove

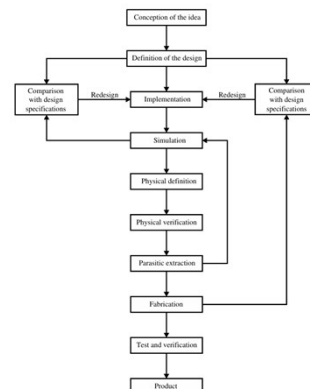


Figure.2 Analog IC design flow

Background

Decoding brain signals for the purpose of neuror rehabilitation and assistive technologies has become one of the central challenges in modern neuroengineering. Non-invasive electroencephalography (EEG) remains one of the most widely used modalities due to its safety, portability, and suitability for long-term monitoring in real-life settings. EEG signals are inherently low signal-to-noise, highly variable across subjects, non-stationary, and therefore requires high-quality signal acquisition. International research on EEG-based systems increasingly emphasizes the importance of dedicated, application-specific AFE circuits to support reliable biosignal acquisition in constrained environments.

Objectives

The overall aim of the project is to develop, implement, and validate an analog front-end signal acquisition circuit for neuromorphic computing architecture and integrate it into the NeuroMate assistive rehabilitation platform for validation.

Method

The project will follow an integrated workflow that begins with the exploration and benchmarking of analog front-end architectures and topologies suitable for EEG-based intention detection. Following the analog IC design flow from specification to IC post-layout simulation, the design will be sent out for tape-out. A custom PCB test board will be designed for post-fabrication evaluation of the IC's performance. The validated AFE IC will be integrated with the neuromorphic processor and embedded electronics, enabling end-to-end real-time operation.