Institute of Mechanical and Electrical Engineering

A 65-nm Frequency-Selective Shared-Channel AFE With Dual-Band Gain for Concurrent EEG and Electrode–Skin Impedance Monitoring

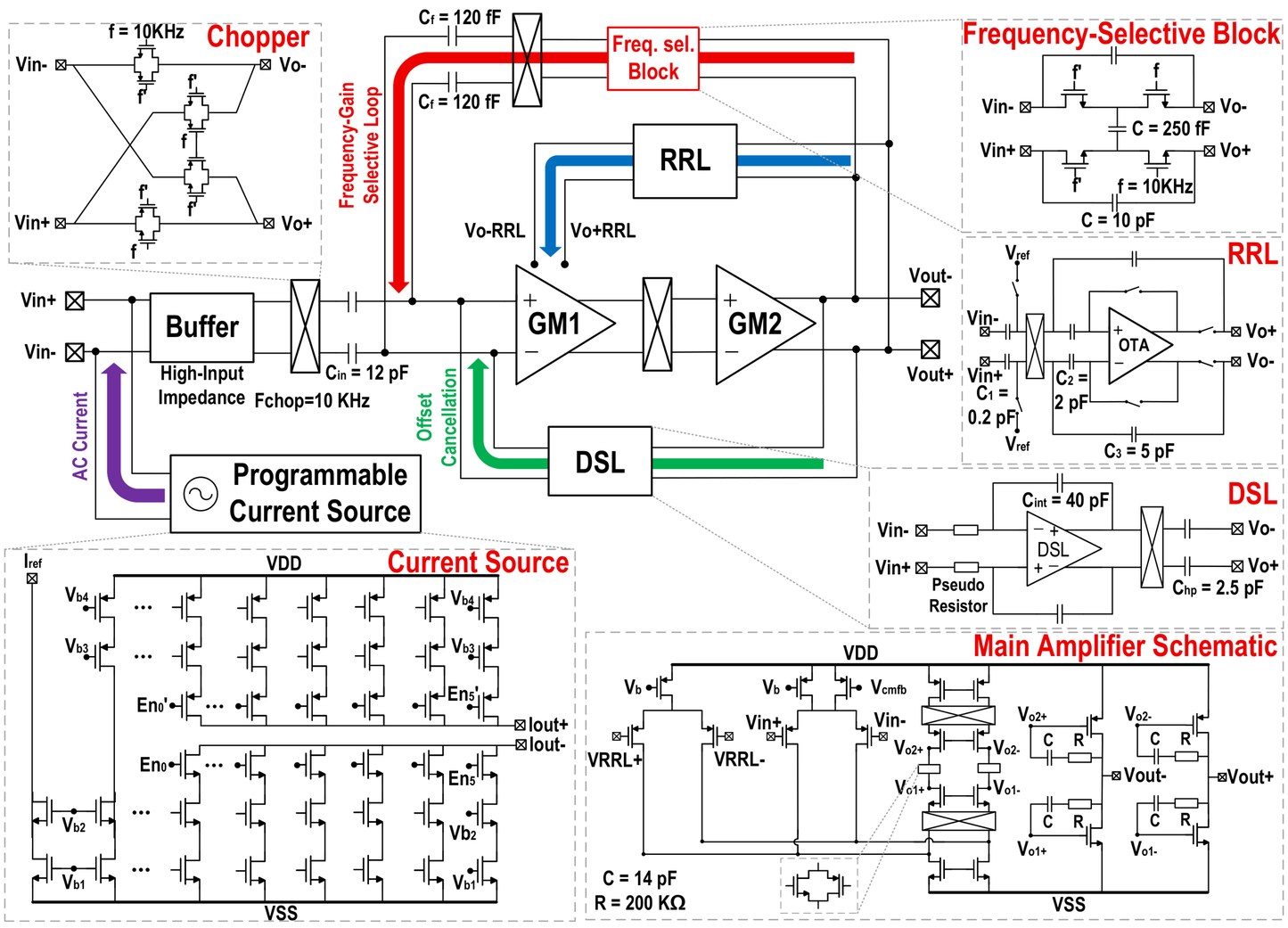
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One analog path, two gain levels: 40 dB for EEG and 20 dB for ESI (electrode–skin impedance).

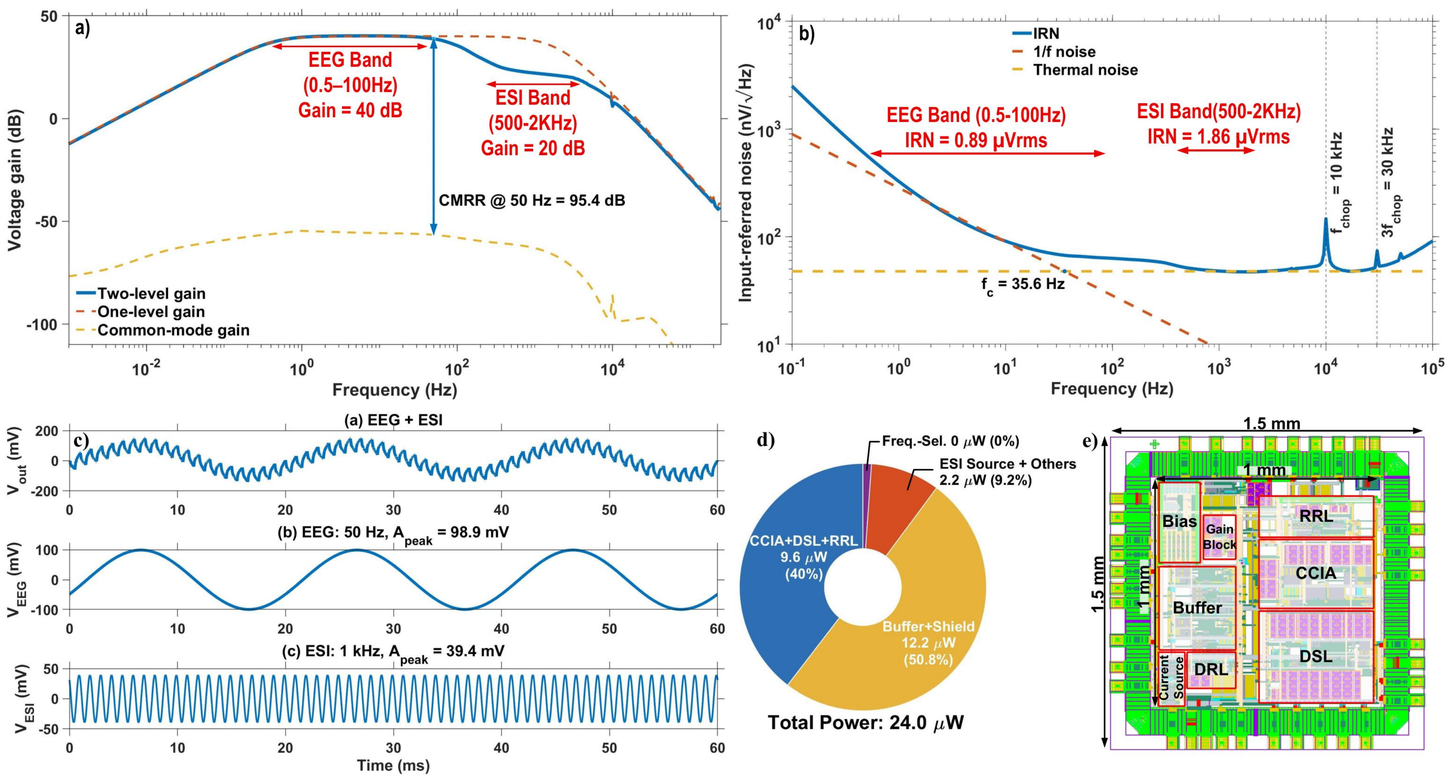
Frequency-selective gain preserves EEG sensitivity while providing headroom for the larger ESI signal, enabling continuous electrode-contact monitoring during EEG acquisition.

Shared EEG–ESI architecture



Chopper-stabilized CCIA with DC servo loop (DSL), ripple-reduction loop (RRL), input buffer and programmable ESI excitation.

Post-layout simulation results



(a) Dual-band gain and common-mode gain. (b) Input-referred noise. (c) Concurrent EEG + ESI. (d) Power breakdown. (e) 65-nm layout.

Supported by the European Union's research and innovation programme under Marie Skłodowska-Curie grant agreement No. 101118964.

Why frequency-selective gain?

EEG requires high gain, but a larger ESI voltage can saturate the shared readout.

Example: 10 nA through 1 MΩ produces 10 mV at the input. A 40-dB gain gives 1 V, while 20 dB limits the output to 100 mV.

Circuit implementation

CCIA: Cin = 12 pF, Cf = 120 fF
Chopping frequency: 10 kHz
Switched-capacitor gain network
Pole near 80 Hz
6-bit DAC: 10–630 nA, 10-nA steps
Input buffer with active shielding

Performance summary

Parameter	Two-level mode
Supply / power	1.2 V / 24 μW
EEG gain / band	40 dB / 0.5–100 Hz
ESI gain / band	20 dB / 500 Hz–2 kHz
EEG input noise	0.89 μV RMS
Input impedance	0.8 GΩ at 50 Hz
CMRR	95.4 dB at 50 Hz
DC-offset tolerance	±100 mV
Circuit area[1]	0.92 mm²

[1] Excludes I/O pads and clamp blocks.
Power includes the input buffer and shield driver.

Concurrent acquisition

50-Hz EEG: 98.9 mV peak output
1-kHz ESI: 39.4 mV peak output
Both signals remain below saturation.

Enabling dual-band gain increases EEG noise only from 0.84 to 0.89 μV RMS.

Conclusion

A shared readout supports concurrent EEG and ESI monitoring at 24 μW. Compared with an estimated duplicated-CCIA implementation, it reduces power by 16.1% and circuit area by 16.4%.[2]

[2] Circuit-based estimates, excluding additional supporting circuitry and routing.