Electrical Properties of Organic Nanofibers and Thin Films

NanoSYD
Mads Clausen Institute
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Images on front page:

Upper left: Fluorescence microscope image of PPTPP nanofibers on KCl substrate.
Upper right: Atomic force microscope image of PPTPP nanofibers on KCl substrate.
Lower left: Schematic illustration of an Organic Field-Effect Transistor (OFET).
Lower right: Brightness-enhanced optical photograph of light emission from an OFET.
Center: A portion of para-hexaphenylene crystal.
Preface

This is my Master Thesis, which is a report of my study and experiment carried out in NanoSYD, University of Southern Denmark (SDU) from February 1 to June 2, 2009. This thesis contains 30 ECTS, and has been written under the supervision of Jakob Kjelstrup-Hansen. Electrical properties of two organic materials were investigated in this Master project based on Organic Field-Effect Transistor (OFET) platform, and the platforms were mainly fabricated in the cleanroom of SDU, Sønderborg, while the electrical measurement was carried out in the optical laboratory of Nanofiber A/S. The project SPRO 8, which I have finished in January 2009, is served as the pre-project of this semester’s work, and the platform fabricating techniques have been improved based on the previous SPRO 8 project.

A number of people have helped me a lot during this Master project. First of all, I would like to thank my supervisor Jakob Kjelstrup-Hansen, who has showed me the entire process of fabricating platforms and gave me important knowledge of organic materials, theoretically and experimentally. I also would like to thank Henrik H. Henrichsen, who is from Technical University of Denmark (DTU), and he made a special instrument which facilitated light emission measurement for samples in vacuum, leading to somehow a breakthrough of my project. Manuela Schiek prepared several samples of organic thin films and nanofibers for me, and also showed me how to introduce monolayer on sample surface. I really appreciate her help. Kasper Thilsing-Hansen gave me many advices on operating various instruments in cleanroom. Roana Melina de Oliveira showed me how to change organic materials in the oven of the high vacuum deposition system and also gave me good advice on how to deal with the system when an unexpected accident happened. I benefit a lot from Morten Madsen’s introduction of using the high vacuum deposition system during my SPRO 8 project as well. Finally, I also would like to express my gratitude to Stefan Johansen, who helped me to make a stand for photo multiplier tube (PMT) in workshop, and Horst-Günter Rubahn, who helped me to set up the PMT. Although the PMT was not used in this project due to some inconvenience, it gave me a better understanding of some important parameters relevant to light emission from organic materials.

Xuhai Liu

Date
## Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>AC voltage</td>
<td>Alternating-Current voltage</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscope</td>
</tr>
<tr>
<td>α-Si:H</td>
<td>Hydrogenated Amorphous Silicon</td>
</tr>
<tr>
<td>BBL</td>
<td>Poly(benzobisimidazobenzophenanthroline)</td>
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<tr>
<td>BCB</td>
<td>Benzocyclobutene</td>
</tr>
<tr>
<td>BC/BG</td>
<td>Bottom Contact/Bottom Gate</td>
</tr>
<tr>
<td>BC/TG</td>
<td>Bottom Contact/Top Gate</td>
</tr>
<tr>
<td>bHF</td>
<td>Buffered hydrofluoride acid</td>
</tr>
<tr>
<td>BPE-PTCDI</td>
<td>N,N'-bis(2-phenylethyl)perylene-3,4:9:10-bis-(dicarboximide)</td>
</tr>
<tr>
<td>DC voltage</td>
<td>Direct-Current voltage</td>
</tr>
<tr>
<td>EQE</td>
<td>External Quantum Efficiency</td>
</tr>
<tr>
<td>F8BT</td>
<td>Poly(9,9-di-n-octylfluorene-alt-benzo[b]thiazole)</td>
</tr>
<tr>
<td>HMDS</td>
<td>Hexamethyldisilane</td>
</tr>
<tr>
<td>HOMO</td>
<td>Highest Occupied Molecule Orbital</td>
</tr>
<tr>
<td>HTP</td>
<td>Hexathiapentacene</td>
</tr>
<tr>
<td>IQE</td>
<td>Internal Quantum Efficiency</td>
</tr>
<tr>
<td>LCD</td>
<td>Liquid Crystal Display</td>
</tr>
<tr>
<td>LUMO</td>
<td>Lowest Unoccupied Molecule Orbital</td>
</tr>
<tr>
<td>NTCDI-C8F</td>
<td>N,N'-di((terfluorohexyl)-1,4,5,8-naphthalenetetracarboxylic diimide</td>
</tr>
<tr>
<td>OFET</td>
<td>Organic Field-Effect Transistor</td>
</tr>
<tr>
<td>OLED</td>
<td>Organic Light-Emitting Diode</td>
</tr>
<tr>
<td>OLEFET</td>
<td>Organic Light-Emitting Field-Effect Transistor</td>
</tr>
<tr>
<td>OTS</td>
<td>Octadecylchlorosilane</td>
</tr>
<tr>
<td>P3HT</td>
<td>Poly-3-hexylthiophene</td>
</tr>
<tr>
<td>p6P</td>
<td>Para-hexaphenylene</td>
</tr>
<tr>
<td>PE</td>
<td>Polyethylene</td>
</tr>
<tr>
<td>PET</td>
<td>Perylene (1,12-b,c,d) thiophene</td>
</tr>
<tr>
<td>PMMA</td>
<td>Poly(methyl methacrylate)</td>
</tr>
<tr>
<td>PPTPP</td>
<td>2,5-bis (4-biphenylyl) thiophene</td>
</tr>
<tr>
<td>PTCIDI</td>
<td>Perylene tetracarboxylic diimide</td>
</tr>
<tr>
<td>PTCIDI-C8H</td>
<td>Dioctyl-3,4,9,10-perylene tetracarboxylic diimide</td>
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<tr>
<td>PVA</td>
<td>Poly-vinyl alcohol</td>
</tr>
<tr>
<td>PVP</td>
<td>Poly-4-vinyl phenol</td>
</tr>
<tr>
<td>RT</td>
<td>Room Temperature</td>
</tr>
<tr>
<td>SAM</td>
<td>Self-Assembled Monolayers</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>TC/BG</td>
<td>Top Contact/Bottom Gate</td>
</tr>
<tr>
<td>TCNQ</td>
<td>Tetracyanoquinodimethane</td>
</tr>
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# Table of Contents

Chapter 1  Introduction ............................................................................................................. 1

Chapter 2  Materials: Phenylene/Thiophene Molecules ................................................................. 3
  2.1 Para-hexaphenylene (p6P) .................................................................................................. 3
    2.1.1 Structure of p6P Oligomer ..................................................................................... 3
    2.1.2 Formation of p6P Nanofibers on Muscovite Mica ............................................... 5
    2.1.3 Band Structure of the p6P Crystal ........................................................................... 6
  2.2 2,5-bis (4-biphenylyl) thiophene (PPTPP)........................................................................... 7

Chapter 3  Platforms: Organic Field-Effect Transistors (OFETs) .................................................... 10
  3.1 Device Configurations ..................................................................................................... 10
  3.2 Principles of OFETs ....................................................................................................... 11
  3.3 Unipolar and Ambipolar OFETs .................................................................................... 15
    3.3.1 p-Channel OFETs .................................................................................................. 15
    3.3.2 n-Channel OFETs .................................................................................................. 16
    3.3.3 Ambipolar OFETs .................................................................................................. 17
  3.4 Crucial Factors in the Type of Transport Channel .............................................................. 18
    3.4.1 Role of Electrodes .................................................................................................. 18
    3.4.2 Role of Dielectric Layer ....................................................................................... 20
    3.4.3 Role of Environment ............................................................................................ 22

Chapter 4  Potential Applications: Organic Light-Emitting Field-Effect Transistors .............. 23
  4.1 Drawbacks of Si-based Light-Emitting FET ...................................................................... 24
  4.2 Unipolar OLEFETs ......................................................................................................... 25
  4.3 Ambipolar OLEFETs ...................................................................................................... 26
    4.3.1 Direct-Current (DC) Gated Ambipolar OLEFETs .................................................. 26
    4.3.2 Alternating-Current (AC) Gated Ambipolar OLEFETs ......................................... 28
    4.3.3 Other Operating Possibilities of AC Gated OLEFETs ........................................... 29
  4.4 Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE) .............. 32

Chapter 5  Preparative Work for Experiments ............................................................................ 33
  5.1 Fabricate chips in Cleanroom .......................................................................................... 33
  5.2 Organic Materials Deposition and Transfer ...................................................................... 34
    5.2.1 Deposition of p6P and PPTPP Thin Films ........................................................... 34
    5.2.2 Deposition of p6P and PPTPP Nanofibers ........................................................... 36
    5.2.3 Wire Bonding, Sample Storage and Sample Groups Classification ....................... 38

Chapter 6  Electrical Experiments (I – V Measurement) ................................................................. 39
  6.1 Experimental Setup and Circuit Check ............................................................................. 39
  6.2 Field Effect Measurement of p6P and PPTPP Thin Films .............................................. 40
    6.2.1 Measurement Circumstances Dependence ........................................................... 40
    6.2.2 Device Degradation in Ambient Air ......................................................................... 41
    6.2.3 Channel Length Dimension Dependence ............................................................. 44

Chapter 7  Optical Experiments (Emission Intensity Measurement) ............................................. 49
  7.1 Experimental Setup ......................................................................................................... 49
  7.2 AC Gate Voltage Powered Light Emission from p6P and PPTPP thin films .................. 50
    7.2.1 Light Emission at the Edge of p6P Thin Films ....................................................... 50
7.2.2 Frequency-dependent Emission Intensity .......................................................... 51
7.2.3 Gap Size-dependent Emission Intensity .......................................................... 52
7.2.4 Emission Difference between p6P and PPTPP Thin Films ..................................... 53
7.2.5 Measurement Circumstances Dependence ....................................................... 54
7.2.6 Sample Degradation and Damage ................................................................. 54
7.2.7 Light Emission from Individual Electrode ....................................................... 56

7.3 Light Emission Investigation of p6P Nanofibers .............................................. 57

Chapter 8 Conclusion and Outlook ....................................................................... 59

Appendix A: Illustration of Several PPTPP molecule orbitals ......................... 61
Appendix B: Derivations of Charge Mobility ....................................................... 62
Appendix C: Description of Chips Fabricating Processes in Cleanroom ............. 64
Appendix D: Optimized Parameters for Wire Bonding Machine ...................... 68
Appendix E: Summary of Sample Groups ............................................................ 69
Appendix F: Calculation of Applied AC Gate Voltage .................................. 70
Appendix G: Sample Holder ................................................................................ 71
Appendix H: Sample Damage after Light Emission Measurement ...................... 72
References ........................................................................................................... 74
Chapter 1  Introduction

Organic nanofibers and thin films built of planar conjugated molecules have attracted great interest due to their promising application potential in future optoelectronic devices, such as organic light-Emitting diode (OLED) \cite{1,2}, solar cells \cite{3} and field-effect transistors (FETs) \cite{4}. These conjugated molecules, such as phenylenes, thiophenes and co-phenythiophenes can result in high charge carrier mobility in electronic devices due to face-to-face or edge-to-face $\pi$-stacking between neighboring molecules (See Fig 2.4 and 2.8). An attractive research direction is to realize semiconductor devices based on such organic materials, which can combine electrical functions and optical functions. Large area active-matrix OLED display is one of such devices that have been commercialized \cite{2}. Light-emitting FETs are also promising in this field, but unfortunately no product based on light-emitting FETs has been mass-produced. However, light-emitting FETs are expected to be superior to OLED, in that the planar configuration of FETs is more suitable for light emitting compared with the vertical structure of OLED. Although the investigation of light-emitting FETs is still at an early stage, inspiring outcome has been fulfilled by a number of research groups. Since the first light-emitting FET based on tetracene thin films is reported by a German group in 2003 \cite{5}, the light-emitting property of FET has been intensively investigated, which even assists to the development of the first organic ambipolar light-emitting FET \cite{6}. Moreover, a novel method based on alternating-current (AC) gate voltage has firstly powered an FET in 2008 \cite{7}.

The organic materials used in this project are p6P nanofibers and thin films, PPTPP nanofibers and thin films. The organic thin film transistors are prepared by depositing thin films directly onto device substrate in high vacuum, whereas the organic nanofiber transistors are prepared by transferring pre-deposited nanofibers onto device substrate. The investigation was intended to focus on PPTPP nanofiber transistors and PPTPP thin film transistors. However, the deposition system for PPTPP materials had not been ready until April 16\textsuperscript{th}, so p6P materials devices were measured mostly during this period. The experiment part is generally divided into electrical experiment and light emission measurement. Obvious field effect from back gate on organic thin films is obtained in electrical experiment, which can be used to calculate charge carrier mobility. For the light emission measurement part, AC gate voltage is mainly applied to OFET; blue light and green light are observed from p6P thin films and PPTPP thin films, respectively. This novel method using AC gate voltage has the possibility to enhance the performance of OLEFETs (Organic Light-Emitting Field-Effect Transistors) substantially.

The aim of Chapter 2 is to give a general introduction of the organic materials utilized in this project. The physical structures of p6P and PPTPP oligomers together with their energy levels are introduced in Chapter 2, which also presents crystal formed by these oligomers.

Chapter 3 introduces the platform for the optoelectronic investigation of this thesis, including the classification of various device configurations, the operating principles of OFETs, the types of charge transport channels as well as critical factors influencing the channels. The unipolar OFET is the major representative of this discussion. In light of its potential important applications, the principle of ambipolar OFET is also briefly depicted in this chapter, in spite that no relevant experiment has been carried for DC voltage gated ambipolar OFET in this project. The charge carrier mobility calculation for unipolar OFET can be found in corresponding appendix.
Chapter 3 mainly aims at the theoretical foundation of the electrical measurement for OFET, whereas Chapter 4 introduces the theory part for the optical measurement, which includes normal DC gated unipolar and ambipolar OLEFETs, as well as the assumed operating principles of AC gated OLEFETs.

The preparative work for the optoelectronic experiments is outlined in Chapter 5, which acts as the bridge from the theoretical discussion to the relevant experiments. It presents a full-scale description of OFET fabrication processes, from the blank chips to the integration of final samples into measurement circuits. This chapter also provides several notices during the sample-fabrication procedure, which might facilitate and improve future fabrication and OFET operation. The classification of sample groups is listed in the appendix of this chapter.

Chapter 6 summarizes the outcome of electrical experiments for OFETs. This chapter highlights the field-effect properties of p6P and PPTPP thin films, together with relevant materials degradation investigation.

For the light emission investigation, only AC gate voltage powered OLEFETs are utilized. Various factors which could affect the total light emission intensity for one OFET device are compared and analyzed in Chapter 7. The brightest AC gated OLEFET obtained in this project has channel length of 2.5µm and 60nm p6P thin films deposited on 200nm SiO₂. Fig 1.1 illustrates its original appearance together with a brightness-enhanced image.

![Fig 1.1: (a) Optical image of an AC gated OFET, captured by Infinity 1 with four second exposure; (b) Corresponding image with enhanced brightness generated by ImageJ.](image)

The theoretical and experimental parts are summarized in the last chapter. Possible future investigation methods and highlights are also proposed in Chapter 8.
Chapter 2  Materials: Phenylene/Thiophene Molecules

The active organic materials utilized in this project are p6P thin films and nanofibers, as well as PPTPP thin films and nanofibers. This chapter introduces the physical structure of these molecules together with their electronic structures. The way how a large number of individual molecules are arranged to form a crystal is also depicted. Since the exact crystal structure of PPTPP in nanofiber geometry on a substrate, such as muscovite mica, is not known, only its crystal structure in macro-scale solution-grown nanofibers is presented.

2.1 Para-hexaphenylene (p6P)

In this section, the physical structure of the p6P oligomer is first introduced, which is followed by the description of how the p6P nanofibers are formed on muscovite mica. The band structure of a p6P crystal is also presented.

2.1.1 Structure of p6P Oligomer

One p6P oligomer can be visualized as a chain of six benzene rings, with a carbon atom in one benzene ring bonded with a carbon atom in another ring. The other carbon atoms bond with hydrogen atoms, as shown in Fig 2.1. For an isolated carbon atom, the electron configuration outside the nuclei of the atom is (1s)² (2s)² (2p)². For a carbon atom in a benzene ring or in p6P oligomer, the two electrons in 2s orbital and one of the two electrons in 2p orbital are hybridized to three electrons in sp² orbital, with the remaining of only one electron in 2p orbital, and the electron configuration in this case is (1s)² (sp²)³ (2p)¹.[8]


Fig 2.2 only illustrates hybrid orbitals of two neighboring benzene rings of one p6P oligomer. For simplicity, the orbitals of ten hydrogen atoms are also omitted. The 2p orbital is indicated in red, which represents both of the phases of the orbital wave function here. Otherwise, a large number of figures are needed to describe various arrangements of wave function phases. When the 2p orbital which is perpendicular to the oligomer plane is bonded with a neighboring 2p orbital, it is called a π bond. The sp² orbital is represented by white and its different wave function phases can be distinguished by different sizes of the torus-shape clouds. When the three sp² orbitals of
one carbon atom are bonded along the orbital axes, they are called σ bonds. The σ bond is usually stronger than the π bond, in that the overlap of two sp\(^2\) orbitals is considerably in excess of that of two 2p orbitals in parallel.

![Fig 2.2: Schematic illustration of hybrid orbitals for two connected benzene rings. Color indication: Red: 2p orbital. White: sp\(^2\) orbital.](image)

It should be noted that the π bond does not necessarily always exist between two 2p orbitals, otherwise the valence electrons should be localized. In fact, all of the valence electrons for one p6P oligomer are delocalized, which enables p6P oligomer to have a lower energy state compared with occupying localized electrons. To specify, one carbon atom possesses four valence electrons, while one hydrogen atom has only one. Therefore, an individual p6P oligomer with 36 carbon atoms and 26 hydrogen atoms occupies 170 valence electrons in total, all of which are delocalized around the oligomer. The state of the delocalized electrons can be described by Molecule Orbital theory\(^9\). It is well known that one molecule orbital can contain two electrons. Thus, one p6P oligomer with 170 valence electrons has 85 occupied molecule orbitals. The molecule orbital with highest energy among the occupied molecule orbitals is called highest occupied molecule orbital (HOMO); while the molecule orbital with lowest energy among the unoccupied molecule orbitals is called lowest unoccupied molecule orbital (LUMO). Fig 2.3 illustrates the HOMO and LUMO of one p6P oligomer generated by ArgusLab 4.0.1, which indicates that the two ends of the oligomer possess less charge density compared with the center part, corresponding to the fact that the electrical conduction mainly occurs along the center part between two neighboring p6P oligomers.
Chapter 2 Materials: Phenylene/Thiophene Molecules

2.1.2 Formation of p6P Nanofibers on Muscovite Mica

The hydrogens around the oligomer can be regarded as being positively charged due to the relative high electronegativity of carbon atoms in the inner part of the oligomer. Thus, Coulomb interaction occurs when two p6P oligomers approach to each other, leading to herring bone-like crystal structure if more oligomers are taken into account. For p6P crystals, it might lead to high enough speed of electrical conduction due to edge-to-face alignment manner of two neighboring oligomers (See Fig 2.4), in which the \( \pi \)-orbital overlaps among different oligomers are facilitated. However, it could be better if two neighboring molecules align in a face-to-face way, which could further increase the \( \pi \)-orbital overlaps, thus high performance of devices based on p6P materials. And it has been simulated that halogen groups are capable of enhancing such \( \pi \)-orbital overlaps \([10]\). It could be a possibility to make p6P derivatives in which the \( \pi \)-orbital overlaps are promoted.

As shown in Fig 2.4, the growing direction of the crystal is not completely perpendicular to the oligomer axis, with an angle of approximately 76° in between \([11]\). Besides, the surface of one p6P oligomer attached to the mica substrate has in fact a tilt angle of 5°, which is not depicted in Fig 2.4. The dashed arrow indicates the axis of p6P oligomer, and the solid arrow indicates the growing direction of crystal, both of which lie in the (1 -1 -1 ) plane. Fig 2.4 only illustrates a small portion of one segment of p6P nanofiber. If oligomers are stacked in the direction of inward or outward of the page, they are linked by weaker Van der Waals force.

Apart from the stack manner of p6P oligomers, the substrate muscovite mica plays an important role for growing ideal p6P nanofibers. For the substrates with reduced interaction with p6P molecules, the molecules tend to stack along the (1 0 0) face, indicated by red plane in Fig 2.4, resulting in layers of upright molecules \([11]\). In contrast to such substrates, the surface of muscovite mica has relatively high interaction with p6P molecules due to being positively charged and polar after cleavage. The p6P nanofiber dimension is normally several ten nanometers in height, several hundred nanometers in width and several micrometers in length. A sample with 5nm p6P nanofiber emitting polarized light after exposure to UV light is illustrated in Fig 2.5, which also depicts the two growing directions of p6P nanofibers on muscovite mica, with an angle of 120° in between.

Fig 2.3: (a) Highest occupied molecule orbital (HOMO) of one p6P oligomer. (b) Lowest unoccupied molecule orbital (LUMO) of one p6P oligomer.
Fig 2.4: A small portion of a p6P crystal. Dashed arrow: the axis of p6P oligomer. Solid arrow: the nanofiber axis. Both of the arrows lie within the (1 -1 -1) plane.

Fig 2.5: Fluorescence microscopic image of 5nm p6P nanofibers. The white arrows indicate two growing directions of p6P nanofibers on the surface of muscovite mica.

2.1.3 Band Structure of the p6P Crystal
HOMO (Highest occupied molecule orbital) and LUMO (Lowest unoccupied molecule orbital) for organic semiconductors are counterpart concepts of the valence band and conduction band for
Chapter 2  Materials: Phenylene/Thiophene Molecules

inorganic semiconductor. Fig. 2.6 (a) is a convenient representation of the energy level of p6P crystal. The symbols $I$ and $A$ represent ionization energy and electron affinity, respectively. The symbols $\Phi$ and $\Phi_m$ represent work functions of p6P crystal and the metal which will be in intimate contact with p6P crystal, whereas $E_F$ and $E_{Fm}$ are respectively the Fermi level of the crystal and metal.

![Energy level diagrams](image)

Fig 2.6: Schematic diagram of energy level of p6P crystal, as well as the energy level change due to contact with metal. (a) A simplified energy level representation of p6P crystal. (b) Energy level diagrams of a metal and p6P crystal before contact. (c) Energy level diagrams of a metal and p6P crystal in intimate contact.

When a p6P crystal and a metal are brought into intimate contact from a relative long distance, major carriers will flow from one material to the other and the Fermi levels of both materials tend to be equal. As charge carriers flow to the other material, a positive space charge on one side and a negative space charge on the other side of the interface set up, and finally a potential barrier is formed, which builds an interface dipole to prevent any further flow of major carriers. Besides, this interface dipole will introduce a vacuum level shift $\Delta$, as illustrated in Fig 2.6 (c). If a downward shift is defined as negative, the barrier height for holes and electrons can be expressed as:

$$
\phi_h = I - \phi_m - \Delta 
$$

(Equation 2.1)

$$
\phi_e = \phi_m - A + \Delta 
$$

(Equation 2.2)

In this case, it is assumed that the major carriers are holes, so the barrier height of hole is increased by the absolute value of $\Delta$. This is not ideal for the p6P semiconductor based FET, because if the barrier is too high, the carriers are mostly limited by inject from the metal to semiconductor, meaning a large operating voltage is needed in order to make the carriers inject into the semiconductor.

### 2.2 2,5-bis (4-biphenyl) thiophene (PPTPP)

One PPTPP oligomer is hybridized by one thiophene and four phenylenes, with two phenylenes on each side of the thiophene. As the dashed circle in Fig 2.7 (a) illustrate, the valence electrons of PPTPP oligomer are also delocalized. Unlike p6P oligomer, the faces of four phenylenes and the face of one thiophene are not in the same plane even in the solid state \([12]\), as shown in Fig 2.7 (b). The HOMO and LUMO calculation of PPTPP oligomer is also carried out using ArgusLab 4.0.1. Since it is significantly complex to calculate the molecule orbitals of a portion of crystal structure...
using ArgusLab due to the complexity of the model itself, only the HOMO, HOMO-1, LUMO and LUMO+1 orbitals of a PPTPP oligomer are depicted in Appendix A. The charge density could be varied dramatically if consider the whole crystal structure, therefore the results provided in Appendix A is only served as showing the distribution of wave functions of the corresponding molecule orbitals, which also indicates the electrical conduction is more likely to take place in the center part instead of two ends among various molecules. The HOMO and LUMO levels of a much more complicated crystal structure could be calculated utilizing relatively advanced software, such as Accelrys Material Studio/Dmol\cite{13}.

Fig 2.7: (a) Top view of a PPTPP oligomer. (b) Side view of a PPTPP oligomer.

The oligomers in PPTPP crystal structure take bent and zigzag shapes, as illustrated in Fig 2.8, which also shows the nanofiber axis, indicated by a solid arrow. The exact alignment parameters, such as tilt angle of bottom oligomers with respect to substrate, of PPTPP crystal on various substrates are still being investigated. However, it has been concluded that the PPTPP nanofibers tend to grow on muscovite mica and KCl satisfactorily\cite{14}. The nanofibers are aligned nearly in parallel along single direction on muscovite mica, which can be explained by a combination effect of molecules/surface-electric-field electrostatic interaction and epitaxy. And the two direction alignment on KCl substrate can be due to epitaxy alone, as shown in Fig 2.9.
Fig 2.8: Illustration of a portion of PPTPP crystal. Solid arrow: indicates the growth direction of PPTPP crystal.

Fig 2.9: (a) AFM image of PPTPP nanofibers on muscovite mica, captured by tapping mode with a scan area 10μm×10μm. The mean height and width of the nanofiber are respectively 45nm and 600nm. (b) PPTPP nanofibers on KCl, captured by tapping mode with a scan area 5μm×5μm. The mean height and width of the nanofiber are respectively 160nm and 440nm.
Chapter 3 Platforms: Organic Field-Effect Transistors (OFETs)

In this Chapter, three OFET configurations are first introduced, followed by the introduction of its operation principle, including the derivation of charge mobility and threshold voltage from experimental current – voltage characteristics. The charge carriers transport channels are classified based on the behaviors of holes and electrons. Finally, several factors which could have critical influences on carriers transport channels are discussed, such as various metal electrodes possessing different work function, an inappropriate dielectric layer which could cause plenty of traps for electrons, and the contamination from operating environment. Besides, the active organic layers presented in this chapter are all represented by organic thin films instead of organic nanofibers, so as to make the introduction more understandable.

3.1 Device Configurations

The most often used OFET configurations are the Bottom Contact/Bottom Gate (BC/BG), Top Contact/Bottom Gate (TC/BG), and Bottom Contact/Top Gate (BC/TG) configurations.

The BC/BG and TC/BG configurations, which are illustrated in Fig 3.1 (a) and Fig 3.1 (b) respectively, have been widely applied since the beginning of the OFET investigation near the end of 20th century. They are also respectively named coplanar structure and staggered structure [15].

For the Bottom Contact/Bottom Gate (BC/BG) configuration, highly doped Silicon is served as substrate, which is directly treated as back gate. A thin dielectric layer which normally consists of SiO₂ is formed on top of the Si substrate. Metal electrodes are then deposited on the dielectric layer using standard optical lithographic process and the metal deposition process, plus lift-off. Finally the active organic layer is deposited onto the dielectric structure. By doing so, the metal electrodes contact with the active organic layer from bottom, thus it is called Bottom Contact configuration. It differs from the Top Contact/Bottom Gate (TC/BG) configuration, in which the metal electrodes touch the active organic layer from top, hence the designation of Top Contact.

Another characteristic of TC/BG structure is that the metal electrodes can not be fabricated by optical lithographic process; otherwise the organic layer could be destroyed.

Both of the above two structures have advantages and disadvantages. The BC/BG configuration is easier and more efficient to fabricate due to the lack of electron beam deposition
technique, but the interface between dielectric and organic layer is limited within the channel sandwiched by the parallel electrodes, and charge carriers are only able to inject from the side walls of electrodes. In contrast, as for the TC/BG structure, the charge carriers can inject from the bottom of the metal electrodes instead from side walls. Since the area of the electrode side walls is much smaller that contacting with the organic layer, it makes sense that the injection resistance of the TC/BG configuration could be less than BC/BG configuration, which has been firstly proved by Steet et al \cite{15}. However, the drawback of TC/BG configuration is that the contact area between organic layer and metal electrodes could be to some extent damaged due to the collision between hot gold atoms and soft organic layer during metal deposition process \cite{16}. And it is obviously less efficient because of involving electron beam deposition process.

Given the respective virtues and shortcomings of BC/BG and TC/BG configurations, it seems apparent that the Bottom Contact/Top Gate (BC/TG) structure, which is shown in Fig 3.1 (c), could avoid all the above mentioned problems of the first two device configurations. The charge carriers can not only inject from the side walls of metal electrodes, but also from the upper parts of the electrodes that overlap with the top gate electrode. Besides, since the source and drain metal electrodes are fabricated before the active organic layer is deposited or spin coated, the collision problem leading to damage of soft organic layer in TC/BG configuration could be overcome. However, SiO$_2$ can not be chosen as dielectric in this case, in that the active organic layer can not be treated with Si oxidation. Instead, organic dielectric is often spin-coated onto the organic layer \cite{17}.

The Bottom Contact/Top Gate (BC/TG) configuration is firstly applied by Zaumseil et al \cite{17}. A conjugated material F8BT with high photoluminescence efficiency of about 50% is utilized as the active organic layer. Ambipolar transport is easily obtained and the external quantum efficiency (EQE) of the resulting emission is 0.75%, which is regarded as the highest EQE of ambipolar OFET ever achieved until the end of 2007 \cite{18}.

In light of the limiting time of this master project and complexity of fabricating TC/BG and BC/TG structures, the BC/BG configuration is chosen to be the platform to investigate the electrical properties of organic nanofibers and thin films.

### 3.2 Principles of OFETs

In this section, the Bottom Contact/Bottom Gate (BC/BG) configuration is only taken into consideration for the convenience of discussion, and associated values such as carrier mobility in the other two configurations can be extracted based on the same principle and process.

Fig 3.2 (a) is the schematic structure of one chip which is used as the platform to investigate different organic materials. The highly doped Si with a thickness of 525 µm acts as bottom gate. A 200 nm layer of dielectric SiO$_2$ is oxidized onto the Si substrate in advance. Titanium/Gold (2nm/30nm) electrodes are then fabricated by standard optical lithographic and metal deposition process, which is followed by the organic film deposition process in high vacuum deposition system. It should be mentioned that the back gate is made to be connect with peripheral circuit by contacting with a rectangular titanium/gold (10nm/50nm) electrode on top of the chip. This electrode is deposited onto Si substrate immediately after the upper SiO$_2$ in this area is etched by buffered hydrofluoric acid. It is important to note that the resistance between drain and source electrode is much larger than that between gate and electrode, which indicates that the leakage
current between drain and source can be neglected, as calculated in Equation 3.1 and 3.2.

\[
R_{gs} = \rho \cdot \frac{d}{A} = 10^{12} \Omega \cdot m \times \frac{200nm}{1.375mm^2} \approx 1.455 \cdot 10^{11} \Omega \quad \text{(Equation 3.1)}
\]

\[
R_{ds} = \rho \cdot \frac{L}{A'} = 10^{12} \Omega \cdot m \times \frac{10\mu m}{1400\mu m \cdot 200nm} \approx 3.57 \cdot 10^{16} \Omega \quad \text{(Equation 3.2)}
\]

where \( R_{gs} \) and \( R_{ds} \) are respectively the gate-source and drain-source resistance, \( \rho \) is the resistivity of SiO\textsubscript{2}, \( d \) the thickness of SiO\textsubscript{2}, \( A \) is the planar area of one metal electrode, \( L \) is the channel length (take 10\( \mu \)m for instance), \( A' \) is the cross section area from drain to source (take one channel for instance).

The grounded electrode is normally called source, while the other comb-structured electrode, to which a certain voltage is applied, is referred to as drain. The selection of source or drain is arbitrary because of their completely symmetrical areas. The potential difference between drain and source is usually denoted by \( V_{ds} \).

Voltage is also applied to gate, and the potential difference between gate and source is denoted by \( V_{g} \). For p-type channel, in which the majority carriers are positively charged holes, a negatively biased gate voltage \( V_{g} \) can accumulate holes at the SiO\textsubscript{2} and organic semiconductor interface, provided that the drain is also biased negatively so as to make holes inject from source. Likewise, for n-type channel, in which the majority carriers are negatively charged electrons, a positively biased gate voltage can then induce electrons at the interface, provided that the drain is also biased positively so as to make electrons inject from source. The accumulated carriers are then able to induce current from source to drain. According to basic capacitance defining equation, the number of charge carriers is proportional to capacitance and potential difference between two sides of the capacitor. Therefore, in this case the number of accumulated carriers per unit area (\( Q_{i} \)) is proportional to the capacitance of dielectric per unit area (\( C_{i} \)) and the gate voltage, which is represented by Equation 3.3.

\[
Q_{i} = C_{i} \cdot V_{g} \quad \text{(Equation 3.3)}
\]

However, since there are always carrier traps at the interface of dielectric and semiconductor, desirable source to drain current could not be achieved unless a certain number of charge carriers firstly sacrifice to fill the traps. The effect of traps could be regarded as a virtual potential difference, namely the threshold voltage \( V_{t} \). Therefore, a higher gate voltage than the threshold voltage is required. Then, the Equation 3.3 should be modified into Equation 3.4.

\[
Q_{i} = C_{i} \cdot \left( V_{g} - V_{t} \right) \quad \text{(Equation 3.4)}
\]

where \( V_{g} - V_{t} \) can be referred to as the effective gate voltage.
Small portions of drain–source channel from Fig 3.2 (a) are illustrated in Fig 3.2 (b) – (d), which show the different operating regimes of the OFET. Channel length is represented by L. And W stands for the channel width, which should be summed up from all the channels in Fig 3.2 (a); the thickness of dielectric is represented by d.

In Fig 3.2 (b), which represents the linear regime, opposite charges form at gate and source when a biased voltage $V_g$ is applied to the back gate. If the charges at the source are injected into the organic semiconductor, and then they are able to spread over the dielectric and semiconductor interface, which can next be drifted from source to drain if an appropriated biased voltage is applied to drain. When the drain to source voltage $V_{ds}$ is much smaller than the gate voltage $V_g$, the potential in the channel increases linearly from source ($V = 0$) to drain ($V = V_{ds}$), the drain to source current $I_{ds}$ is proportional to $V_{ds}$, and $I_{ds}$ is determined by Equation 3.5.

$$I_{ds} = \frac{W}{L} \cdot C_i \cdot \mu_{lin} \cdot \left(V_g - V_t\right) \cdot V_{ds}$$

(Equation 3.5)

where W and L are channel width and channel length, respectively, $C_i$ is the dielectric capacitance per unit area, $\mu_{lin}$ is the charge mobility in linear regime. Since the drain to source current $I_{ds}$ is proportional to $V_g$, the mobility can be derived from the slope of $I_{ds}$ versus $V_g$ at constant $V_{ds}$ as Equation 3.6 shows.
As the drain to source voltage $V_{ds}$ increases further, finally leading to the potential difference between gate and drain being equal to the threshold voltage $V_t$, a depletion region then forms at the drain, which is illustrated by Fig 3.2 (c). The local potential at the pinch-off line in this case is $V_{ds,sat}$, which equals to $V_g - V_t$.

If the drain to source voltage is further increased, the potential difference between gate and drain will be less than the threshold voltage, resulting in widening the depletion region, which is shown in Fig 3.2 (d). However, the local potential at the pinch-off line remains $V_g - V_t$, therefore the potential difference between this line and the source is unchanged. This is called the saturation regime. It should be noted that a space-charge limited current can flow across the depletion region by the high electrical field in this region [19]. The drain to source current in saturation regime can be given by Equation 3.7.

\[
I_{ds,sat} = \frac{W}{2L} \cdot C_i \cdot \mu_{sat} \cdot (V_g - V_t)^2
\]

(Equation 3.7)

It can be seen from the above equation that the square root of $I_{ds,sat}$ is proportional to gate voltage $V_g$, and the relation between the square root of $I_{ds,sat}$ and gate voltage $V_g$ can be plotted as a straight line. The threshold voltage $V_t$ can then be determined by the intersecting point of the straight line with $V_g$ axis. And the slope of this line is used to calculate the charge mobility in the saturation regime.

The detailed derivations of Equation 3.5 and Equation 3.7 are presented in Appendix B.

The denotations of device parameters in this section are suitable for both p-type channels and n-type channels. But the signs of parameters must be treated with meticulous care when different types of channels are taken into account. Both the n-channel and p-channel enhancement mode together with their linear and saturation regime illustrations are shown in Fig 3.3.

Fig 3.3: Enhancement mode for organic semiconductor. (a) n-channel enhancement mode, electrons are major charge carriers. (b) p-channel enhancement mode, holes are major charge carriers.
thickness of dielectric, namely \( L > 10d \), so as to avoid the influence of lateral field from drain to source voltage on the field created by gate voltage \([19]\). Besides, the channel width should be at least ten times larger than the channel length, i.e. \( W > 10L \) in order to minimize the fringe current effects flowing outside the channel \([20]\).

### 3.3 Unipolar and Ambipolar OFETs

In the previous section, only the principle of a unipolar OFET is discussed based on the BC/BG device configuration. Apart from unipolar OFETs, ambipolar OFETs have also been under intensive investigation by several research groups from Switzerland, Italy, USA and UK since 2004 \([6][21][22]\). However, the study of ambipolar OFETs is still at its early stage compared with the initial investigation on p-channel OFETs in 1964 \([23]\) and on n-channel OFETs in 1990 \([24]\).

In this section, the research development and respect major characteristics of p-channel and n-channel unipolar OFETs are introduced at the beginning, in terms of their highest charge mobility, processed method as well as organic materials in crystalline form such as nanofibers. Finally, the operating principle of ambipolar OFETs is briefly presented, though it is not investigated in the experimental part of this Master project due to limiting time.

#### 3.3.1 p-Channel OFETs

For p-channel FETs, the major charge carries are positively charged holes, which seem to be less vulnerable to the surface state of semiconductor/insulator interface compared with electrons. The development of p-channel OFETs is more advanced than the n-channel counterpart before the end of 20th century.

Since the first field effect on small organic molecules Cu-phthalocyanine is demonstrated in 1964, the first value of hole mobility \( 1.5 \times 10^{-5} \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) from Merocyanine had not been reported until 1984 \([25]\). Among the organic materials, pentacene seems to be the most excellent molecules which can result in hole mobility of up to \( 2.4 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \). The article reporting this fundamental limit of hole mobility from organic thin films was withdrawn due to academic misconduct in 2002. However, the previously reported hole mobility had already surprisingly been \( 1.5 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) in 1997 \([26]\), which is comparable to inorganic materials, such as hydrogenated amorphous silicon (\(\alpha\)-Si:H) with hole mobility of \( 5.1 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) \([27]\). But pentacene thin films can only be vacuum deposited due to its low solubility.

Materials which could be solution processed are more suitable for large-scale p-channel FET fabrication, which facilitate manufacturing procedures and finally lower cost. The solution processable organic materials Poly-3-hexylthiophene (P3HT) has the highest hole mobility to date, up to \( 0.1 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) \([28]\).

The above mentioned values of hole mobility are all obtained from thin films, no matter vacuum deposited or solution processed. However, higher hole mobilities can be expected in corresponding crystalline forms because of lower molecule disorder and almost no impurities in crystal. For instance, the solution processed hexathiapentacene (HTP) single-crystal nanowires exhibit hole mobility up to \( 0.27 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \), which is six times larger than that of vacuum deposited HTP thin films \([29]\). And so far, the largest hole mobility obtained from solution processed organic crystals is \( 1.42 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \), reported by Kim et al. in 2007 \([30]\). When it comes to vacuum deposited nanowires, the same principle holds as well. It is reported that vacuum deposited nanowire
transistors from perylo (1,12-b,c,d) thiophene (PET) possess hole mobility of 0.8 cm$^2$V$^{-1}$s$^{-1}$, which is almost ten times more than that of PET thin films [31]. And Menard et al. reported the largest hole mobility from vacuum deposited rubrene single crystals, which is 20 cm$^2$V$^{-1}$s$^{-1}$[32].

### 3.3.2 n-Channel OFETs

In contrast to p-channel FETs, electrons are the major charge carriers in n-channel FETs. Owing to the instability of organic anions which can easily react with oxygen or water molecules in the ambient air and its relatively large vulnerability to traps at the semiconductor/insulator interface, satisfactory performance of the n-channel FET is harder to achieve. The development of n-channel OFETs seems to be always far away lagging behind the p-channel OFETs during the past decade. However, the need of fabricating electronic elements such as voltage inverter boosts investigations of n-channel OFETs. And studying the n-channel transport could also compare with p-channel device performance and elucidate transport mechanism thoroughly.

For the organic thin film n-channel transistors, Guillaud et al. reported the first n-channel OFET with electron mobility of 2×10$^{-4}$ cm$^2$V$^{-1}$s$^{-1}$ from Pc$_2$Lu in 1990 [24]. However, the n-channel behavior was only observed under vacuum condition at room temperature. No n-channel behavior was obtained upon exposure to ambient air. C60 devices also exhibit similar performance, ant its electron mobility could reach to 0.3cm$^2$V$^{-1}$s$^{-1}$ in vacuum but quickly decreased 4-5 orders of magnitude in ambient air [33]. The largest electron mobility from vacuum-sublimated organic thin film reported to date is 0.6 cm$^2$V$^{-1}$s$^{-1}$ of PTCDI-C8H, which is a derivative of PTCDI, by Malenfant [34]. After that, no reported electron mobility could exceed this value even organic dielectric such as PVA was used. And it should be mentioned that vacuum deposited thin films has normally larger electron mobility compared with solution processed thin films regarding the same materials. For instance, vacuum deposited NTCDI-C8F has electron mobility up to 0.1 cm$^2$V$^{-1}$s$^{-1}$, while only 0.01 cm$^2$V$^{-1}$s$^{-1}$is obtained for solution processed device [35], which might due to the non-uniform films achieved by solution processed method.

Like p-channel OFETs, the active organic materials in the crystalline form for n-channel OFETs has more excellent performance compared with corresponding thin film devices. The first n-channel single-crystal OFET is based on tetracyanoquinodimethane (TCNQ), with electron mobility up to 1.6 cm$^2$V$^{-1}$s$^{-1}$ [32]. A novel solution processed method to fabricate n-channel nanowire FETs has been come up recently by Hak Oh et al. and a surprising electron mobility 1.4 cm$^2$V$^{-1}$s$^{-1}$ of a BPE-PTCDI single-crystalline organic microwire was obtained [36]. And such PTCDI derivatives are considered as the most promising organic materials with n-channel characteristics. Briseno et al. has reported that PTCDIs nanowires with electron mobility on the order of 10$^{-2}$ cm$^2$V$^{-1}$s$^{-1}$, and more inspiringly, they have utilized such nanowires to successfully fabricate the first complementary inverters based on one-dimensional organic semiconductor [37], as shown in Fig 3.4. The source of the n-transistor is grounded and the source of the p-transistor is connected with power supply. The drains of two transistors are linked and served as output. The advantage of such inverters consisting of p-channel and n-channel OFETs is to minimize the leakage current during operation, in that only one transistor, p-channel or n-channel, is turned on when the output is in a steady logic state, which can be seen in Fig 3.4 (c). This could significantly reduce the power consumption compared with inverters constituting of only one type of transistor.
It is also amazing that the stability of n-channel transistors in ambient air has been under intensive investigation and considerable improvements have been reported. The mostly recently exciting progress is from Briseno et al., and they have fabricated n-channel OFET based on poly(benzobisimidazobenzophenanthroline) (BBL) nanobelts with electron mobility up to $7\times10^{-3}$ cm$^2$V$^{-1}$s$^{-1}$, which exhibit stable and reproducible performance in ambient air for six months [38]. Besides, the mechanical properties of organic nanowires or nanofibers are being studied as well [29] [39].

For clarity, the reported highest charge carrier mobility for p-channel and n-channel OFETs are summarized in Table 3.1.

It can be optimistically predicted that large-scale-fabrication-suitable solution processed, high mechanical property possessed, ambient air stable OFETs consisting of thin films or crystals could be fulfilled in future.

<table>
<thead>
<tr>
<th></th>
<th>Thin Film</th>
<th>Crystal</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vacuum-deposited</td>
<td>Solution-processed</td>
</tr>
<tr>
<td>p-channel</td>
<td>1.5</td>
<td>0.1</td>
</tr>
<tr>
<td>n-channel</td>
<td>0.6</td>
<td>Not reported</td>
</tr>
</tbody>
</table>

Table 3.1: Summarization of highest charge mobility for p-channel and n-channel OFETs fabricated through vacuum deposition and solution process. Unit: (cm$^2$V$^{-1}$s$^{-1}$).

### 3.3.3 Ambipolar OFETs

The above mentioned complementary inverters composed of both p-channel and n-channel transistors are complicated to fabricate due to involving additional manufacturing steps, thus
higher production cost. Therefore, ambipolar OFETs exhibiting both n-channel and p-channel characteristics could overcome this problem. Besides, through the simultaneous injection of electrons and holes with almost equal mobilities, it can be conclude that the electron transport in organic materials may not be necessarily inferior to holes, which could shed new light on the charge carriers transport mechanism of OFETs [40].

The device configuration of ambipolar OFETs can be the same of that of unipolar OFETs. Take Fig 3.2 (a) for example, which is Bottom contact/Bottom Gate structure, assume that the source is grounded and apply a positive gate voltage $V_g$, which is equal to applied positive drain to source voltage $V_{ds}$, i.e. $V_g = V_{ds}$. Since the gate is positively biased with respect to the source, electrons are injected from source and then induced through the semiconductor/insulator layer by $V_{ds}$, if the gate voltage is larger that the threshold voltage of electrons, $V_g > V_{t,e}$.

Next, if the gate voltage $V_g$ is reduced to a value less that the threshold voltage of electrons, it is obvious that no electrons inject from the source. At the same time, the gate voltage has been negatively biased with respect to the drain due to reduced value, therefore holes can be injected from the drain, if the absolute value of difference between drain and gate is larger than the absolute value of the threshold voltage of holes, i.e. $|V_g - V_{ds}| > |V_{t,h}|$. It should be noted that the threshold voltage of holes is a negative value, so absolute value is taken into consideration when discussing the transport of holes.

However, if the gate voltage $V_g$ is reduced to a level that is still larger than the threshold voltage of electrons in the above step, i.e. $V_g > V_{t,e}$, whereas maintain the condition that the threshold voltage of holes can also be overcome, i.e. $|V_g - V_{ds}| > |V_{t,h}|$, then both of holes and electrons are injected into the semiconductor/insulator interface, leading to light emission if other conditions are also satisfied.

### 3.4 Crucial Factors in the Type of Transport Channel

As mentioned in section 3.3, the investigation of p-channel OFETs was carried on much earlier and more widely until recently than n-channel OFETs, which is partly because excellent n-channel devices are more difficult to be obtained owing to its instability and many factors that could have considerable influences on them. And these factors can also affect p-channel OFETs performance substantially. In this section, various factors which determine the capability of OFETs are introduced, including the type of electrodes, the relative position of electrodes with respect to active organic materials, the effects of dielectric layer and the effects of exposure to ambient air.

### 3.4.1 Role of Electrodes

Assume a piece of organic layer has intimate contact with metal electrodes on both sides, the band structure for the organic layer and two metal electrodes can be simplified as Fig 3.5. Here it is assumed that the two metal electrodes are symmetric. Under biased voltage, the holes could be injected from metal electrode on one side into the organic semiconductor, whereas the electrons could be injected from electrode on the other side into the organic layer, either is unipolar transport. When the electrons and holes are injected from respective electrodes into organic semiconductor simultaneously, it is called ambipolar transport. If the work function of metal electrode is somehow aligned with the LUMO or HOMO level of organic layer well, an ohmic contact is formed at the interface, which can facilitate the charge injection. However, if the work
function of the metal electrode is misaligned too much with the LUMO or HOMO level of the organic layer, a Schottky barrier is formed and the holes or electrons from metal electrodes should surmount this barrier so as to inject into the organic semiconductor. According to Fig 3.5, if the two metal electrodes are symmetric, i.e. they are in the same type, and then at least one charge carriers, electrons or holes, are hard to overcome the relatively high barrier. In that case, large voltage is normally required to help charge carriers inject.

Practically, metal electrodes with high work function, such as Au (5.1eV) and Pt (5.12-5.93), are needed to ease injection of holes into organic layer, while metal electrodes with low work function, such as Mg (3.66) and Ca (2.87), are desirable for the injection of electrons. However, the metal electrodes with low function are generally significantly unstable in ambient air and easy to be oxidized, which could quickly degrade the performance of OFET with such electrodes. This is one reason that limits the early development of n-channel OFETs, because normally more stable metal electrodes with high work function were utilized even for the injection of electrons, and it is obviously no satisfactory results for n-channel transport. This problem could be alleviated by depositing protecting layers on top of completed device so as to prevent the low work function metal electrode from exposing to ambient air. Another straightforward method is to keep the device into vacuum directly. To specify, Sakanoue et al. have reported an alignment-free process to fabricate asymmetric contact electrodes, resulting in much higher drain to source current compared with devices with symmetric electrodes[41]. According to their experiment statement, Al is firstly deposited with an angle of 30° with respect to the surface of substrate, and then Au is deposited with an angle of -30° with respect to the surface of substrate. After liftoff, a series of Al-Au asymmetric electrodes with 1µm channel length are obtained, as shown in Fig 3.6 (b).
In this case, one individual electrode slice with both of Au and Al is treated as source or drain. When drain to source voltage is applied, only the gaps sandwiched by Au source and Al drain emit light, while other gaps stay unlit, as illustrated in Fig 3.6 (a). And the drain to source current gained from such Au-Al electrodes was reported to be 50 times larger than that obtained from normal symmetric Au electrodes with equal channel length. This clearly shows that large drain to source current can be obtained by reducing the injection barriers both for holes and electrons.

The position of electrodes with respect to active organic layer and back gate in the device also plays an important role. As discussed in Section 3.3, in the Bottom Contact/Top Gate (BC/TG) configuration, the charge carriers can not only inject from the side walls of metal electrodes, but also from the upper parts of the electrodes that overlap with the top gate electrode, which could make already known p-channel transport also show n-channel characteristics. It has been reported that an top gate OFET device utilizing F8BT as active organic layer and PMMA as gate dielectric shows ambipolar transport, while a bottom gate device with the same structure elements only exhibits p-channel transport\textsuperscript{[42]}. This indicates that the type of transport channel also relies on specific position of electrodes.

3.4.2 Role of Dielectric Layer
It has been simulated that the charge density of an OFET device is normally confined to the first
several monolayers at the semiconductor/insulator interface \cite{43}. Therefore, the selection of dielectric layer and the consequent quality of interface between organic semiconductor and the dielectric could have a substantial influence on the device performance. Apart from the high barrier for electrons to inject from metal electrode into the organic layer, which has been discussed in Section 3.4.1, another reason why n-channel transport has been previously relatively rare compared with p-channel is the stronger trapping of electrons than holes at the semiconductor/insulator interface. A large amount of electrons that have been injected from metal electrode can be bound with the pervasive hydroxyl groups on the surface of SiO\(_2\), but normally this does not happen to holes.

Chua et al. have demonstrated the improvement of n-channel transport when a hydroxyl-free gate dielectric was used \cite{44}. In their investigation, no n-channel characteristics are observed when SiO\(_2\) was utilized as gate dielectric and Ca as top contact electrodes. However, n-channel transport was immediately obtained when a buffered gate dielectric BCB (Benzocyclobutene) was deposited onto SiO\(_2\). Another buffered gate dielectric PE (Polyethylene) was also tested and functioned similarly to BCB dielectric.

In addition to buffered dielectric layer, self-assembled monolayers (SAMs) of alkylsilanes can alleviate the effects of hydroxyl groups as well. Common alkylsilanes are butyl-, decyl- and octadecylchlorosilane (BTS, DTS and OTS) with alkyl chains of four, ten and eighteen carbon atoms, respectively. The chlorine atoms attached to Si in alkylsilanes can combine with hydrogen atoms of the hydroxyl groups on the surface of SiO\(_2\) and then form hydrochloric acid, and alkylsilanes can consequently be bound onto the SiO\(_2\) surface, thus forming monolayer, as illustrated in Fig 3.7.

![Fig 3.7 Illustration of the formation of alkylsilane SAMs.](image)

The reduction of threshold voltage of n-channel FETs can be attributed to the introduction of such alkylsilanes monolayers. The degree of threshold decrease appears to depend on the length of alkyl chain of the monolayers. The largest reduction of threshold voltage is obtained from devices with OTS as monolayer, while the smallest reduction is observed from devices with BTS as
monolayer. The alkyl chain of OTS is nearly five times longer than that of BTS\textsuperscript{[44]}. It should be noted it seems that the SAMs are less effective than buffered dielectric such as BCB and PE mentioned above, in that the threshold voltage of n-channel devices could be shifted back to higher voltage if the OFET in question is operated for a long time.

In this project, OTS monolayers are applied to several blank chips before depositing active organic layers. A solvent of 50ml requires approximately 0.1ml OTS. Since hydroxyl groups are distributed on the surface of SiO\textsubscript{2} dielectric, solvents with hydroxyl groups, such as ethanol, are not suitable. Toluene (C\textsubscript{7}H\textsubscript{8}) is utilized as solvent in this experiment. The blank chips were immersed in the solution overnight. Before depositing active organic layer on the OTS disposed blank chips, the OTS residues should be cleaned off firstly. Since OTS monolayers have been bonded with the SiO\textsubscript{2} surface tightly, it would no damage the monolayers even sonic agitation is given. Unfortunately, some OTS residues still left on the chips after 30 second sonic agitation in acetone, and then p6P thin films were deposited. The samples with OTS showed no improved performance in terms of the light emission measurement, which might be partly due to the uncleaned OTS residues. This problem should be avoided in future experiment.

Apart from introducing buffered dielectric or SAMs onto SiO\textsubscript{2}, organic gate dielectric is another choice. Poly-4-vinyl phenol (PVP) and poly-vinyl alcohol (PVA) had been chosen as gate dielectric and ambipolar pentacene OFET was realized\textsuperscript{[45]}.

### 3.4.3 Role of Environment

The presence of oxygen and water in the ambient air, if they diffuse into the semiconductor/insulator interface of an OFET, can capture electrons, thus affecting the n-channel behavior. It has been demonstrated that the exposure to ambient air can changes the polarity of OFETs based on titanylphthalocyanine or fullerene from n-channel to p-channel characteristics\textsuperscript{[46][47]}. Sakanoue et al. investigated the effects of air exposure on a single-component ambipolar OFETs based on six different organic materials\textsuperscript{[48]}. They concluded that the mobility of holes could be barely influenced by the exposure to ambient air, while the mobility of electrons could be significantly influenced, which indicates electrons are more vulnerable to oxygen or water in the ambient air. They also concluded that the threshold voltage of p-channel devices could be shifted to a higher value (here the threshold voltage is negative, so higher value means lower absolute value), while the threshold voltage of n-channel was not, which can be explained as the hole density in the organic layer increased due to oxygen capturing electrons, thus a positive shift in the threshold voltage. Similar results are obtained in this project, which is presented in the experiment part, Section 6.2.2.
Chapter 4 Potential Applications: Organic Light-Emitting Field-Effect Transistors

Since the first active-matrix liquid crystal display panel was produced in the United States in 1972 [49], the liquid crystal display (LCD) flat panel has been accounted for a huge global market share. Take the black and white LCD panel for instance, the crystal molecules, which can be rotated by external electric field, are placed in the middle of two polarizing filters in perpendicular directions. And a backlight behind the rear polarizing filter is required to provide light source. When a specific control circuit corresponding to a portion of liquid molecules is not operating, the originally twisted crystal molecules can reduce the polarization of the incident light from backlight source, making the panel appearing grey. When the molecules are affected by an external electric field, the crystal molecules can be rotated so as to totally polarize the incident light, resulting in a black panel appearance. The color LCD display is based on the same principle, except that one pixel on the panel is divided into three subpixels, and each subpixel can be controlled independently to generate a large amount of different color for one pixel. In this case, the backlight source should be always operating no matter whether the twisted crystal molecules are rotated by external electric field or not. This could be summed up to substantial power consumption if a large number of LCD panels are taken into account. Therefore, a device without backlight source is desirable, which is also based on elements that can be controlled by an external circuit.

Organic Light-Emitting Diode (OLED) displays seem to be an ideal candidate. For the basic configuration of an OLED, an individual active organic layer, composing of conductive layer and emissive layer, is sandwiched between cathode and anode. When a voltage is applied between the two electrodes, electrons are injected from the cathode while the anode can withdraw electrons, i.e. inject holes. Therefore, electron and hole recombination occurs at the interface of emissive layer and conductive layer, thus emitting light. It should be noted that the organic layer is not necessarily composed of single element. Rather, multiple organic layers could also be utilized. In this way, the active organic layer emits light independently controlled by an external electric field without any other light source. One disadvantage of OLED display is that the cathode or anode should be transparent so as to allow the generated light to emit outside in a vertical-structure component. First, this limits the selection of electrode. Second, it does not provide an easy access to optical probes to image or characterize the emission directly.

In contrast to OLEDs, the organic light-emitting field-effect transistors (OLEFETs) are constructed in a planar configuration allowing the generated light to emit out, which is superior to OLEDs. Besides, OLEFETs are also based on active organic layers that can emit light independently, so the flat panels consisting of OLEFETs do not need a back light source either. Light-emitting FETs based on inorganic materials, such as silicon or hydrogenated amorphous silicon have been proposed [50]. However, silicon-based FETs are not suitable for light emission due to the indirect band gap of silicon.

In this chapter, the reason why silicon-based FETs are not light-emission efficient is first introduced, in an attempt to compare with the advantages of OLEFETs. The operation principles of unipolar and ambipolar OLEFETs are then presented, together with a brief introduction of internal quantum efficiency (IQE) and external quantum efficiency (EQE).
4.1 Drawbacks of Si-based Light-Emitting FET

For inorganic semiconductor, the emission of photons could be attributed to several mechanisms, such as band-to-band transitions, impurity-to-band transitions, and free-carrier transitions. Only the band-to-band emission is considered here, which can be divided into direct band-to-band emission and indirect band-to-band emission, and both should satisfy two conditions: the conservation of energy and the conservation of momentum\(^{[51]}\).

The conservation of energy means that the energy of one emitted photon \(h\nu\) should be the difference between the energy level of the electron and the energy level of the hole, i.e.

\[
E_2 - E_1 = h\nu \tag{Equation 4.1}
\]

where \(E_2\) is the energy level occupied by the electron involved in the emission of photon, \(E_1\) is the energy level occupied by the hole, \(h\) is the Planck constant \(6.62617 \times 10^{-34} \text{ J} \cdot \text{s}\) and \(\nu\) is the frequency of photon.

The conservation of momentum means that the momentum of the photon is the difference of the momentums of the electron and hole involved in this interaction, i.e.

\[
p_2 - p_1 = \frac{h\nu}{c} \tag{Equation 4.2}
\]

where \(p_2\) and \(p_1\) are the momentum of the electron and hole, respectively, \(c\) is the speed of light in vacuum. Equation 4.2 can also be written as

\[
k_2 - k_1 = \frac{2\pi}{\lambda} \tag{Equation 4.3}
\]

where \(k_2\) and \(k_1\) are the angular wavenumber of the electron and hole, respectively, and \(k = {p/(2\pi h)}\).

The photon momentum magnitude is negligibly small compared with that of electrons and holes. Therefore, the momentum of the electron and hole involved in the interaction can be regarded as being equal, thus \(k_2 = k_1\). This is called the k-selection rule.

As for the direct band-to-band emission, the transition from the bottom of the conduction band to the top of the valence band is likely to happen without any exchange of momentum, as illustrated in Fig 4.1 (a). However, when it comes to the indirect band-to-band emission, the bottom of the conduction band and the top of the valence band do not correspond the same angular wavenumber, as shown in Fig 4.1 (b). This means that the transition is unlikely to happen owing to the requiring exchange of momentum which can not be accommodated by the emitted photon. In this case, phonons must be introduced to assure the momentum to be conserved.
Therefore, silicon, which is an indirect-gap semiconductor, is not suitable for the emission of light.

Another disadvantage of Si-based light-emitting FETs is the high degree of processing, such as high manufacturing temperature, which could possibly be overcome by for example solution processed OFETs.

4.2 Unipolar OLEFETs

The first unipolar OLEFET was demonstrated by Hepp et al. in 2003 [5]. They utilized a Bottom Contact/Bottom Gate (BC/BG) device configuration, with blank chips being silane-coupling-agent treated before depositing tetracene thin films. Gold was chosen to be source and drain electrodes. But gold with a high work function is not suitable for the injection of electrons into organic semiconductor. P-channel characteristic was obtained as previous investigation, but in addition, weak light emission was also observed in the vicinity of drain, which is a clear evidence of the recombination of holes and electrons. The light emission only near to drain could be attributed to the difficulty of electrons to fully inject into organic semiconductor. Therefore, holes injected from the source electrode should move along the entire channel length to arrive at the drain electrode to recombine with much less electrons injected from drain.

It makes sense that if the electrons injection is enhanced, then the recombination of holes and electrons should be improved. However, even asymmetric metal electrodes which facilitate both of electron and hole injection were used by some research groups [52] [53], the light emission of unipolar OFET still occurred only in the vicinity of drain electrode. A triangular tunneling barrier model was proposed by Santato et al. to explain this phenomenon [54]. As shown in Fig 4.2, this model assumes that the HOMO and LUMO level of organic layer are distorted near to the semiconductor/electrode interface by voltage drop. Electrons from the drain electrode can directly inject to the HOMO level of organic material, which, of course, does not contribute to light emission. On the other hand, electrons could only tunnel into LUMO level of organic layer along a barrier with W in length, because the barrier height H is too high to be surmounted. The barrier height H is equal to the difference between HOMO and LUMO level, while the tunneling barrier length is inversely proportional to the drain to source voltage $V_{ds}$. 

![Fig 4.1 (a): Photon emission in a direct-gap semiconductor; (b) Photon emission in an indirect-gap semiconductor.](image-url)
4.3 Ambipolar OLEFETs

In contrast to unipolar OLEFETs, electrons can inject into organic layer like holes in ambipolar OLEFETs, and both of electrons and holes are injected simultaneously with comparable charge mobilities, leading to efficient recombination of charges with two polarities. The emission zone of ambipolar OLEFETs can be controlled by varying gate voltage $V_g$ and drain to source voltage $V_{ds}$.

Apart from the above mentioned ambipolar OLEFETs powered by DC gate voltage, Yamao et al. proposed a novel method based on AC gate voltage in 2008, by which a layer of 300nm PPTPP thin films was lit up [7]. Although their analysis of the emission mechanism based on experimental data seems to be reasonable, the optical image they provided does not have enough resolution to distinguish whether the light emission only occurs within the charge transporting channel or also takes place at other semiconductor/electrode interfaces (See Fig 4.5). Similar experiment was carried on in this project and it turned out that all the interface between organic layer and gold electrode was lit up, which will be discussed in Section 7.2.1 and 7.2.7.

4.3.1 Direct-Current (DC) Gated Ambipolar OLEFETs

As discussed in Section 3.3.3, according to the presence of different charge carriers, three operating regimes can be defined: the unipolar regime for electrons, the unipolar regime for holes and the ambipolar regimes with presence of both electrons and holes. In fact, each unipolar regime could be divided into linear regime and saturation regime. For simplicity, the different operating regimes are only defined based on the presence of charge carriers. It makes sense that the light emission taking place near to the middle of transporting channel would be more intense than that emitted from the semiconductor/electrode interface, in that electrons and holes can recombine sufficiently without influences from metal electrodes. This was firstly proved by Zaumseil et al. using a Bottom Contact/Bottom Gate (BC/BG) configuration with a high photoluminescence efficiency (10%) organic material [22].

In their experiment, Au is used for the source electrode and Ca for the drain. The light emission is visible when the device is operated in ambipolar regime. It starts with a low negatively biased gate voltage $V_g$ and a high negatively biased drain to source voltage $V_{ds}$. In this case, the
drain is much more negative than gate, so electrons inject from the source electrode and dominate the channel, as illustrated in Fig 4.3 (a). It is true that the source electrode is currently more positive than gate, but since the gate voltage begins with a low negatively biased value, the threshold voltage of holes $V_{t,h}$ cannot be complemented so far, thus no injecting holes. Next, the gate voltage $V_g$ is decreased to a more negative value until the threshold voltage of holes $V_{t,h}$ is complemented, then holes start to inject from source electrode, as shown in Fig 4.3 (b). And light emission takes place near the source electrode. Then, as the gate voltage $V_g$ is reduced further (its absolute value is, of course, increasing), the emission line moves from source to drain and vanishes when it arrives at the drain electrode. At the same time, holes dominate the channel, as illustrated in Fig 4.3 (c). And this process is reproducible. It is important to note that the emission intensity stays constant while the emission line moves from one electrode to another, but it decreases when it moves near to electrodes. This can clearly explain and prove the operating mechanism of ambipolar OLEFETs. The maximum external quantum efficiency (EQE) of this device is 0.35%.

Besides, the light emission property of a Bottom Contact/Top Gate (BC/TG) device is also investigated [17]. The organic material F8BT with higher photoluminescence efficiency (50%-60%) is utilized, and the maximum EQE of this device is 0.75%, which is more than twice of the
previous BG/BC device. However, it can not be concluded whether the increase of EQE is due to the substitution with a higher photoluminescence material or due to the change of device configuration.

4.3.2 Alternating-Current (AC) Gated Ambipolar OLEFETs

Unlike DC gated ambipolar OFETs, AC gated OFETs require constant voltage to be applied to source and drain electrodes, and of course, an AC voltage supply connect to the gate electrode. As illustrated in Fig 4.4 (a), negative constant DC voltage $V_s$ is applied to source, which acts as electron injecting electrode, while positive constant DC voltage $V_d$ is applied to drain, which is served as hole injecting electrode. And an AC voltage is applied to the gate electrode, with frequency $f$ and amplitude $V_G$.

![Schematic diagram of the operating circuit of AC gated ambipolar OLEFET.](image)

The amplitude of gate voltage $V_G$ should be larger than $V_d$ and the absolute value of $V_s$, as shown in Fig 4.4 (b). When the AC voltage reaches the bottom of the cycle (Point P1), it is similar to the unipolar situation that the hole injection electrode (drain) is much more positive than gate electrode, therefore holes dominate the channel. When the AC voltage moves to the value that equals to $V_s$ (Point P2), i.e. the potential difference between the source and gate is zero as discussed in Section 3.2, pinch-off line appears. As the AC voltage moves toward positive value (for instance Point P3), the source becomes more negative compared with the gate electrode, and
electrons start to inject from the source. In order to inject enough electrons, the source should be much more negative than the gate electrode, therefore an AC gate voltage with large amplitude is desirable, as mentioned above. If the injected electrons meet with holes at the ‘pinch-off’ line of the hole density profile, the electron-hole recombination takes place and light is emitted.

It is important to note that the frequency of the AC gate voltage should be high enough, in an attempt to assure the injected electrons are adequately rapid to meet with holes, before the holes arrive at the source electrode owing to the fact that a space-charge limited current can flow across the depletion region. Otherwise, only one polarity of charge present within the channel, which is out of the ambipolar regime.

It has been demonstrated by Yamao that the light emission intensity is dependent on the frequency of AC gate voltage and the drain to source voltage\(^7\). According to their experiment, the emitted light from the organic layer blinks when the frequency of the AC voltage is in the range of 2 – 20 Hz, whereas the light is continuous when the frequency reaches 200 Hz. The emission intensity of AC gate voltage is compared with that of DC gate voltage. Even the frequency of AC voltage is as low as 2 Hz, its corresponding emission intensity is much larger than that of DC gate voltage. On the other hand, if the frequency of AC voltage is kept constant and the drain voltage and source voltage are varied synchronously, the light emission intensity is increased when \(V_d\) is made larger, which indicates that larger drain and source voltage facilitate the injection of charges. It is also interesting that emission is observed at high frequency (20 kHz), even the drain and source voltage is zero.

### 4.3.3 Other Operating Possibilities of AC Gated OLEFETs

The brand new method to light up an OFET provided by Yamao throws new light on the light emission mechanism of OFETs. The dependence of emission intensity on the frequency of AC voltage and magnitude of drain and source voltage seems to be well-founded. However, two problems are not very clarified in their work. Firstly, it is hard to distinguish the exact emission area from the optical image they captured due to a low resolution problem, which is shown in Fig 4.5.

---

**Fig 4.5:** (a) Photograph a unlit OLEFET device; (b) The same device emits light in dark (The lit area out of channel is marked by a rectangular frame).\(^7\)
It can be found clearly that the part out of the channel area of the electrode on the right hand side also emits light. The two circles on two sides of the channel area, which could be contact pads of drain and source, are also questionable. It seems that all of the semiconductor/electrode interfaces can emit light. The similar emitting results obtained in this master project are also presented in Chapter 7.

Another problem is that the device is also lit up with $V_d = V_s = 0$V when the frequency of AC gate voltage is high enough, which seems to have nothing to do with the channel length.

A possible explanation to these problems is that an individual electrode can function as both electron injecting electrode and hole injecting electrode. Assume an AC voltage is applied to back gate of an OFET with only one metal electrode, as shown in Fig 4.6 (a). When the AC voltage is operating in the positive regime, an electric field is formed from gate toward metal electrode, and electrons are attracted out of the electrode. Next, when the AC voltage is operating in the negative regime, as illustrated in Fig 4.6 (b), an opposite electric field is formed from metal electrode toward back gate, and holes are attracted from the electrode. However, electrons have been injected into the organic layer in the previous step, which are now driven by the opposite electric field. Therefore, holes injected due to negative gate voltage can meet with electrons previously injected due to positive gate voltage, thus leading to light emission. Fig 4.6 (c) illustrates the electrons and holes accumulation regime corresponding to Fig (a) and (b), $P_a$ and $P_b$ indicates electrons accumulation and holes accumulation, respectively.

It should be mentioned that a DC voltage applied to metal electrode could change the ratio of electrons and holes accumulation regime. For instance, if a negatively biased DC voltage is applied to the metal electrode, the electric field generated by AC voltage operating in positive regime can be enhanced, whereas the electric field generated by AC voltage operating in negative regime can be weakened. Therefore, the central line in Fig (c) can be regarded as moving downwards, resulting in larger electrons accumulation regimes, as shown in Fig 4.6 (d). However, it is complicated to define whether the change of accumulation regime can facilitate electron and hole recombination, in that the recombination is also dependent upon charge carriers mobility. Moreover, if a second metal electrode is taken into consideration, an extra electric field would also play a role, leading to more complex problem. Therefore, a more complicated model and simulation is needed, which could be investigated based on future experiments.
Chapter 4  Potential Applications: Organic Light-Emitting Field-Effect Transistors

Fig 4.6: Illustration of the operating principle of individual-electrode OLEFET. (a) AC gate voltage is in the positive regime; electrons accumulate; the metal electrode indicated in yellow is grounded; the largest arrow shows the direction of electric field. (b) AC gate voltage is in the negative regime; holes accumulate. (c) Illustration of electrons and holes accumulation regime corresponding to Fig (a) and (b); P_e indicates electrons accumulation, P_h indicates holes accumulation. (d) Possible change of accumulation regime due to applying DC voltage to metal electrode.

The experiment result relevant to individual electrode emission is provided in Section 7.2.7. Moreover, since channel length is not of vital importance, all the organic semiconductor/electrode interfaces should emit light, and corresponding experiment result is offered in Section 7.2.1.

However, since clear evidence in Yamao’s work shows that the emission intensity is dependent on the drain and source voltage, and experiment in Section 7.2.3 of this project also shows the channel length dependence, it is believed that two possibilities could co-exist.

Finally, leakage current from gate voltage could also play a role. Delicate simulation is needed to further investigate this complex mechanism.
4.4 Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE)

IQE and EQE are two important parameters to determine the light generation efficiency of a semiconductor material. IQE is defined as the ratio of the radiative hole and electron recombination rate to the total recombination rate, including both radiative and nonradiative processes. And the definition of IQE can be given by the following equation:

\[ \eta_{\text{int}} = \frac{f_r}{f} = \frac{f_r}{f_r + f_{nr}} \quad (\text{Equation 4.4}) \]

where \( f_r \) is the radiative combination rate and \( f_{nr} \) is the nonradiative combination rate.

Since radiative lifetime \( \tau \) is inversely proportional to radiative rate \( f \), and the radiative and nonradiative lifetime \( \tau_r \) and \( \tau_{nr} \) have the following relation,

\[ \frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} \quad (\text{Equation 4.5}) \]

IQE can be rewritten as

\[ \eta_{\text{int}} = \frac{\tau}{\tau_r} = \frac{\tau_{nr}}{\tau_r + \tau_{nr}} \quad (\text{Equation 4.6}) \]

IQE directly indicates the light generation capability of a semiconductor material. However, practically, the generated light could be absorbed within the semiconductor device again, and only a portion of this generated light can go out of the device. EQE determines the scale of the light which can emit out of the device.

\[ \eta_{\text{ex}} = \eta_e \cdot \eta_{\text{int}} \quad (\text{Equation 4.7}) \]

where \( \eta_e \) is the overall transmission efficiency.
Chapter 5 Preparative Work for Experiments

This chapter is served as the bridge from the above theory discussion and the following two chapters relating to experiments. Since the Top Contact/Bottom Gate (TC/BG) configuration involves electron beam deposition which is relatively time-consuming, and the Bottom Contact/Top Gate (BC/TG) configuration is comparatively new structure which requires plenty of test experiment, only the Bottom Contact/Bottom Gate (BC/BG) device platforms are fabricated in cleanroom applying standard optical lithographic process. Section 5.1 presents the selection of the mask for electrodes and back gate connecting pad, together with the introduction of chips fabricating process in appendix C. Section 5.2 describes the deposition of p6P thin films and PPTPP thin films as well as deposition and transfer of respective nanofibers. The method of how to deposit thin films more efficiently using carbon tab is also depicted in this section.

5.1 Fabricate chips in Cleanroom

In order to maintain same conditions for electrons injecting electrode and holes injecting electrode, it is reasonable to utilize a lithographic mask with symmetric electrode shadows for one chip. Apart from the same areas of two electrodes on one chip, a much longer channel width than channel length is desirable in an attempt to minimize fringe current effects. Therefore, an interdigitated structure of electrodes is required so as to make the summation of channel width. Fig 5.1 is a capture from a mask layout generated by L-Edit, showing the interdigitated electrode structures with 50 µm, 25 µm and 10 µm gaps from left to right, respectively. The dimension of each chip is 3 mm long and 5mm wide. The channel width is accumulated to 2.66 cm for each chip. The 10 µm gap can not be distinguished by eye in this figure due to short gap compared to the other two chips. And it seems that the 25 µm gaps are not of the same size at different locations in the middle chip, which, however, is merely due to eye illusion. The chips with gap sizes of 5 µm, 2.5 µm and 1.5 µm are not illustrated here.

The back gate mask shadows are 700 µm × 1600 µm rectangular, which are intended to another electrode mask. Therefore, when the electrode locations have been patterned on a wafer using electrode mask and the marks on the wafer and on the subsequent back gate mask are superposed, the back gate mask should be displaced laterally without any rotation to the middle of the source and drain electrode square pads, in an effort to gain a final chip layout as shown in Fig 3.2 (a).

Practically, it does not make remarkable difference whether the electrodes or the back gate pads are fabricated in the first place. But, since the back gate pads are of vital importance to determine the influence of back gate on the charge transport channel, it is safer to make electrodes firstly so as to minimize the exposure of back gate during the fabricating process. However, its exposure to air would not have any bad influence on the chip quality after the entire lithographical processes are finished.

The wafer fabrication processes in cleanroom are introduced in Appendix C, which is based on the process used in the project of the last semester, namely SPRO 8. And a number of improvements have been made in this Master project and added into Appendix C, which could be helpful for fellow students who will make substrates in cleanroom in future.

The processed wafer is taken out of cleanroom and diced using a dicing saw machine in
basement. The remaining thickness of the wafer is optimized to 150 µm (the wafer is 525 µm in thickness), which can be easily broken manually but is not prone to break by itself.

Finally, the diced wafer is carried back to cleanroom carefully and is separated manually there. The resulting chips with different gap dimensions are stored and ready to be used in various standard rectangular boxes in cleanroom.

![Image of interdigitated electrodes with source and drain of equal areas. From left to right, channel length: 50 µm, 25 µm and 10 µm.](image)

### 5.2 Organic Materials Deposition and Transfer

The intended highlighted investigation object for this master project is PPTPP (2,5-bis (4-biphenyl) thiophene) thin films and nanofibers. However, the deposition system for PPTPP materials had not been ready until after April 16th, namely two months since this project begun. During this period, p6P (Para-hexaphenylene) thin films and nanofibers are focused to be investigated in terms of field-effect characteristics and light emissions driven by AC gated voltage. After April 16th, several samples with 32nm PPTPP thin films are briefly tested both electrically and optically. And 5nm PPTPP nanofibers are deposited on two muscovite mica and one KCl samples, which, however, are not measured due to limiting time. Nevertheless, the experiment outcomes from p6P materials are related tightly to the future PPTPP closer investigation.

In this section, the deposition of p6P and PPTPP thin films as well as p6P nanofibers are presented, together with a brief discussion of PPTPP nanofibers deposition. Several steps such as chips storage and wire bonding before integrating the chips into measuring circuits are introduced. Finally, the various chip groups intended for respective electrical and optical measurement are listed for clarity.

#### 5.2.1 Deposition of p6P and PPTPP Thin Films

Both of the p6P and PPTPP thin films are deposited using high vacuum deposition system. Although there are two such systems respectively intended to p6P and PPTPP deposition in the optical laboratory at NanoSYD, the basic principle and the operating procedures as well as the main deposition parameters remain the same. Since the sample holder of p6P deposition system is able to carry more individual chips and this system is more often utilized in this master project, the following thin films deposition processes are introduced assuming the p6P deposition system is being used.
The blank chips must be cleaned before being put into vacuum chamber. The cleaning procedures are carried out in cleanroom, firstly applying thirty seconds sonic agitation to the chips which are immersed in acetone, followed by isopropanol immersion and DI water rinse. It is highly recommended to put the cleaned chips into deposition chamber immediately after cleaning. It is tested that the cleaned chips act as normal uncleaned chips after being stored in standard storage box for four days.

In order to deposit thin films on as more chips as possible for one deposition cycle, two semicircular carbon tabs are stuck onto the sample holder, which then carry several blank cleaned chips, as shown in Fig 5.2. Since the sample holder is kept at room temperature (RT) while depositing thin film, unfriendly objects to the vacuum chamber such as carbon tab can be utilized in this case. All the back gate pads are then covered by plastic-like foil. Otherwise, if thin films are also deposited on the back gate pads, undesirable short circuit could happen when voltage is applied to different terminals.

![Fig 5.2: Chips arrangement on the surface of sample holder.](image)

The major depositing parameters both for p6P and PPTPP thin films are listed in Table 5.1 as follows:

<table>
<thead>
<tr>
<th></th>
<th>p6P thin films</th>
<th>PPTPP thin films</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base pressure (mbar)</td>
<td>$2.2 \times 10^{-8}$~$1.1 \times 10^{-7}$</td>
<td>$7.0 \times 10^{-7}$</td>
</tr>
<tr>
<td>Holder supply (A)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Holder temperature (°C)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Oven supply (A)</td>
<td>2.2 ~ 2.24</td>
<td>Not recorded</td>
</tr>
<tr>
<td>Oven temperature (°C)</td>
<td>395 ~ 410</td>
<td>240~255</td>
</tr>
<tr>
<td>Deposition rate (Å/s)</td>
<td>0.1~0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Thickness (nm)</td>
<td>100; 60; 24.</td>
<td>32</td>
</tr>
</tbody>
</table>

Table 5.1: Depositing parameters for p6P and PPTPP thin films.

The oven supply and oven temperature for p6P thin films are given as a range, because p6P thin films with various thickness are deposited, and each time these two parameters are not the same.
It is also interesting that the 100 nm thick p6P thin films appear green, while p6P and PPTPP thin films with other thickness appear purple blue, which might because certain wavelengths exhibit destructive interference and are therefore not observed in the reflected light \[^{[55]}\].

### 5.2.2 Deposition of p6P and PPTPP Nanofibers

The nanofibers are deposited on muscovite mica and then transferred to cleaned blank chips. PPTPP nanofibers are also deposited on KCl substrate. If the freshly cleaved mica is exposed in ambient air for a long time, for example more than an hour, the mica could not be used anymore. It is appropriate to put the mica in the depositing vacuum chamber at once after cleaving.

Unlike depositing thin films, the sample holder for nanofibers should be heated in advance before heating the oven. The depositing parameters for p6P and PPTPP nanofibers are provided in Table 5.2:

<table>
<thead>
<tr>
<th></th>
<th>p6P nanofibers</th>
<th>PPTPP nanofibers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base pressure (mbar)</td>
<td>(3.2 \times 10^{-8})</td>
<td>(2 \times 10^{-8})</td>
</tr>
<tr>
<td>Holder supply (A)</td>
<td>0.5</td>
<td>2.0</td>
</tr>
<tr>
<td>Holder temperature (°C)</td>
<td>157</td>
<td>87</td>
</tr>
<tr>
<td>Oven supply (A)</td>
<td>1.2 (\rightarrow) 2.2</td>
<td>Not recorded</td>
</tr>
<tr>
<td>Oven temperature (°C)</td>
<td>388</td>
<td>237~255</td>
</tr>
<tr>
<td>Deposition rate (Å/s)</td>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>Thickness (nm)</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 5.2: Depositing parameters for p6P and PPTPP nanofibers.

The formation and final quality of nanofibers on mica have much to do with many critical factors, such as base pressure of depositing vacuum, temperature of sample holder and oven, depositing thickness as well as the quality of mica itself. The p6P nanofibers deposited in this project are not long and separate enough compared with those in the last semester, which might be owing to the substitution with a new sample holder while keeping exactly the same depositing parameters, or because of long exposure (approximately half an hour) of cleaved mica in the ambient air. The PPTPP nanofibers deposited using another deposition system both on mica and KCl are of good quality. Due to small temperature difference on the sample holder of this depositing system, the characteristics of PPTPP nanofibers on the same mica differs at different positions. Fig 5.3 shows fluorescence microscope images of PPTPP nanofibers on mica and KCl.
Fig 5.3: Fluorescence microscope images of PPTPP nanofibers on mica (a), (b) and on KCl (c)

The three images of Fig 5.3 are all taken by 50× optical lens. According to Fig 5.3 (a) and (b), the sizes of PPTPP nanofibers at different positions on the same mica substrate differ greatly. The nanofibers in (b) are relatively near the center of the heating source, so these nanofibers are more separate and long.

The displacement of nanofibers from mica to other platforms is always a significant challenge for the investigation of electrical properties of nanofibers, in that the shape, the length and the whole quality of nanofibers could be notably affected during the transferring process. Besides, the nanofibers are very vulnerable to contamination during this process as well.

One method to transfer nanofibers involves a mechanical instrument with the mica on, which is then pressed onto targeting platform manually. The nanofibers can hardly remain intact in this way. Moreover the metal electrodes with thickness in nanometer scale could also be damaged. New transferring method has been conceived and tested by Kasper Thilsing-Hansen at NanoSYD.
Chapter 5 Preparative Work for Experiments

The nanofiber status after transfer is compared in Fig 5.4. Although the magnifications of optical lenses are not the same between Fig 5.4 (a) and (b), it can be safely concluded that the new transferring method is much superior to the other.

![Fig 5.4 (a): p6P nanofibers transferred manually. (b) p6P nanofibers transferred by new method (Imaged by Kasper Thilsing-Hansen).](image)

### 5.2.3 Wire Bonding, Sample Storage and Sample Groups Classification

The deposited samples are then glued to sample carriers and wire bonded. It should be noted that it is not recommended to wire bond all the deposited chips at a time. It is appropriate to wire bond only one and then measure the electrical characteristics of this sample at once, keeping other samples in closed box. Otherwise, the bonding wires connected with samples might pick up charges from air and influence the sample performance, if they could not be tested in time. Since the bonding wire is significantly fragile, the wire bonding machine is a little bit hard to control. One optimized series of parameters are provided in Appendix D, in which the parameter positions are corresponding to those on the control panel of the wire bonding machine. And the parameters for ‘SEARCH’ are not given, because they have to be adjusted according to the height of holding table. Another tip is that large force and power should be avoided when the bonding tip hit the electrode pads, otherwise the bonding wire might connect with Si substrate, leading to short-circuits.

When it comes to storing the deposited samples, it is strongly recommended to put them in circular box, which is closed or opened by rotating the box lid, rather than keep in much cheaper rectangular box, which should be closed or opened by larger force resulting breaking of the bonded wire. However, considering the relatively high cost of circular boxes and large amount of samples, it could be a good idea to move a series of samples from circular box to rectangular box after measuring. And then the used circular box should be completely cleaned, which can be used again.

For clarity the groups of samples used in this project are summarized in Appendix E, including the gap sizes of various samples and respective active organic materials. The sample 2 in Group 1, for example, is referred to as G1S2.
Chapter 6  Electrical Experiments (I – V Measurement)

The experiment in this chapter is mainly carried on in ambient air. The calculated charge mobilities are about three or four order magnitudes less than previous reports \cite{56,57,45}, which could be due to long exposure of the samples in ambient air. Although the values of mobilities are not as expected, it does show clear field-effect property and the mobilities vary for different channel lengths.

6.1 Experimental Setup and Circuit Check

The major instruments for electrical experiments consist of a Stanford Research SR570 current pre-amplifier, a 16-bit National Instruments DAQ card and a Steuerbares Netzgerat DC voltage amplifier. The schematic diagram of the experimental setup is illustrated in Fig 6.1. The bonded sample is integrated into the circuit by a home-made 6-pin connector. Source and drain electrodes are selected arbitrarily. The source is connected with the input end of SR570 current pre-amplifier, which is grounded; while the drain is connected with the output end of the voltage supply. Since the 16-bit National Instruments DAQ card can only provide a voltage up to 10 volt, the Delta Elektronika voltage supply is needed to multiply the voltage provided by DAQ card by a factor of 20.

Several attentions must be considered carefully. First, the drain to source voltage $V_{ds}$ is normally swept from 0 to -60 volt in this project, so the input voltage applied by DAQ card should be set to -3V. There is high possibility to burn up the DAQ card if the applied voltage is set excessively, for example ±10 volt. Second, the Steuerbares voltage amplifier is only able to output positive voltage; extra cables and connectors should be added into this setup if negative drain to source voltage is required. Next, it is appropriate to apply the drain to source voltage when the DC power supply connected with the gate has been turning on for approximately one minute, otherwise a signal pulse might be obtained at initial points of output curve. Finally, it is of vital importance to note that the compliance current of SR570 current pre-amplifier must be adjusted according to the expected drain to source current $I_{ds}$. To specify, if the anticipated output current from an OFET device is, for instance, in the range of 50 pA to 100 pA, then the compliance current should not be in excess of about 800 pA. The reason is simply similar to the fact that the scale of micrometer can not be measured by a daily ruler with minimum scale of millimeter.
To make sure the whole circuit works well, a commercialized inorganic n-channel transistor BF 245C has been welded to a substrate carrier and integrated into the circuit before real measurement. The output field-effect curves correspond to the information provided by the data sheet of BF 245C.

6.2 Field Effect Measurement of p6P and PPTPP Thin Films

The electrical experiment outcomes of p6P and PPTPP thin films are presented in this section. The sample 3 in Group 2 is used to investigate the measurement difference in ambient air and in vacuum. The samples in Group 5 are with p6P thin films of only 24nm owing to running out p6P powder during deposition. However, the samples in this group are suitable to study degradation. Group 6 is for PPTPP thin films, which exhibit lower threshold voltage compared with p6P thin films.

6.2.1 Measurement Circumstances Dependence

As illustrated in Fig 6.2, apparent p-channel characteristic is obtained. The drain to source current $I_{ds}$ at $V_g = -40\, \text{V}$ is larger than that when $V_g = 0$. When the gate voltage is positively biased, almost zero current is gained in the sweeping range of $V_{ds}$. Fig 6.3 shows the measurement result of the same sample in vacuum. Although the gate voltages are different from the two measurement, the drain to source current $I_{ds}$ at $V_g = -30\, \text{V}$ in Fig 6.3 is more than twice of that at $V_g = -40\, \text{V}$ in Fig 6.2, which clearly indicates larger current is expected if the sample is kept in vacuum.
6.2.2 Device Degradation in Ambient Air

Only 24nm p6P thin film is deposited on G5S1, which is actually an accident owing to the sudden empty of oven during deposition process. Apart from thinner thin films than metal electrode height,
the linear regime provided in Fig 6.4 seems to be notably different from normal curves given in Fig 3.3, so the charge mobility calculated from G5S1 is unlikely to be reasonable. Besides, the transfer characteristics shown in Fig 6.6 and Fig 6.7 indicate respectively clear degradation after $V_g = -50V$ and $V_g = -20V$. Therefore, the magnitude of drain to source current $I_{ds}$ and the shift of threshold voltage are mainly discussed in this section.

For the same sample G5S1, the output characteristics that is measured immediately after deposition is provided in Fig 6.4, and Fig 6.6 illustrates its corresponding transfer characteristics, whereas the output characteristics that is measured on the second day after deposition is presented in Fig 6.5, and Fig 6.7 shows its corresponding transfer characteristics. Comparing the drain to source current values in Fig 6.4 with those at the same $V_g$ in Fig 6.5, it can be easily concluded that the values in Fig 6.5 are higher that their counterparts in Fig 6.4. This could be due to the fact that oxygen and water in ambient air are good electron acceptors, which leads to a larger hole density in organic semiconductor, thus higher drain to source current after longer exposure in ambient air.

Moreover, from Fig 6.6 and Fig 6.7, it can be seen that the onset voltage (similar to threshold voltage) is shifted from -40V in Fig 6.6 to -10V in Fig 6.7, which is in accord with the assumption in Section 3.4.3 that the hole density might be increased due to oxygen acting as electron acceptors.

However, the above analysis does not mean that it is appropriate to expose the samples in ambient air as long as possible, in that degradation seems to be inevitable during prolonged operation. According to Fig 6.5, $I_{ds}$ at $V_{ds} = -60$ when the gate voltage $V_g = -60$ is much less that when $V_g = -50V$, which indicates obvious degradation. Besides, the level-off lines after $V_g = -50$ in Fig 6.6, together with those after $V_g = -20V$ in Fig. 6.7, also show clear degradation, in that otherwise the drain to source current should increase with higher gate voltage.

![Fig 6.4: G5S1 (L = 5µm) p-channel output characteristics measured in ambient air on the 1st day after 24 nm p6P](image-url)
thin films deposition.

Fig 6.5: G5S1 (L = 5µm) p-channel output characteristics measured in ambient air on the 2nd day after 24 nm p6P thin films deposition.

Fig 6.6: G5S1 (L = 5µm) p-channel transfer characteristics measured in ambient air on the 1st day after 24 nm p6P thin films deposition, corresponding to Fig. 6.4.
Chapter 6  Electrical Experiments (I-V Measurement)

Fig 6.7: G5S1 (L = 5µm) p-channel transfer characteristics measured in ambient air on the 2nd day after 24 nm p6P thin films deposition, corresponding to Fig. 6.5.

6.2.3 Channel Length Dimension Dependence

The samples in Group 6 have 32 nm PPTPP thin films, output characteristic with clear linear and saturation regimes are obtained. The output characteristics of G6S8 (with 10µm channel length) and G6S4 (with 1.5µm channel length) are presented in Fig 6.8 and 6.9, respectively. The corresponding transfer characteristics are illustrated in Fig 6.10 and 6.11. According to Equation 3.6, the hole mobilities of G6S8 and G6S4 are calculated as follows:

\[
\mu_{h,G6S8} = \frac{g_{m1, V_{ds}=10} \cdot \frac{L_1}{W} \cdot \frac{1}{C_i} \cdot \frac{1}{V_{ds}}}{633.84(pA/V) \cdot \frac{10 \mu m}{26600 \mu m \cdot 1.73 \times 10^{-8}(F/cm^2) \cdot 10V}} = 1.380 \cdot 10^{-6}\left(cm^2/V \cdot s\right) \quad (Equation \ 6.1)
\]

\[
\mu_{h,G6S4} = \frac{g_{m2, V_{ds}=10} \cdot \frac{L_2}{W} \cdot \frac{1}{C_i} \cdot \frac{1}{V_{ds}}}{526.47(pA/V) \cdot \frac{1.5 \mu m}{26600 \mu m \cdot 1.73 \times 10^{-8}(F/cm^2) \cdot 10V}} = 1.716 \cdot 10^{-7}\left(cm^2/V \cdot s\right) \quad (Equation \ 6.2)
\]

where \(W\) is the channel width, \(L_1\) and \(L_2\) are respective channel length, \(g_{m}\) is the transconductance fitted from \(V_g = -30V\) in transfer characteristics. \(C_i\) is the insulator capacitance per unit area between gate and semiconductor, which is calculated as follows:
\[ C_{i} = \frac{\varepsilon_r \varepsilon_0}{d_{\text{SiO}_2}} = \frac{3.9 \times 8.854 \times 10^{-12} \text{ F/m}}{200 \text{nm}} = 1.73 \times 10^{-8} \text{ F/cm}^2 \]  \hspace{1cm} (Equation 6.3)

where \( \varepsilon_r \) is the dielectric constant of SiO\(_2\), \( \varepsilon_0 \) is the vacuum permittivity, \( d_{\text{SiO}_2} \) the thickness of gate insulator.

Fig 6.8: G6S8 (L = 10\( \mu \)m) p-channel output characteristics measured in ambient air on the 1st day after 32 nm PPTPP thin films deposition.
Fig 6.9: G6S4 (L = 1.5μm) p-channel output characteristics measured in ambient air on the 5th day after 32 nm PPTPP thin films deposition.

Fig 6.10: G6S8 (L = 10μm) p-channel transfer characteristics measured in ambient air on the 1st day after 32 nm PPTPP thin films deposition, corresponding to Fig. 6.8.
Figure 6.11: G6S4 (L = 1.5µm) p-channel transfer characteristics measured in ambient air on the 5th day after 32 nm PPTPP thin films deposition, corresponding to Fig. 6.9.

Equation 6.1 and 6.2 show that the hole mobility of PPTPP thin film calculated from wider channel (10µm) is approximately 8 times larger than that calculated from narrower channel (1.5µm). Similar results are obtained from p6P thin film. It can be explained by a model which involves the metal-semiconductor-interface resistance and the resistance along the channel length. If the drain to source current $I_{ds}$ is determined by contact barrier which can be visualized as the interface resistance, the current is injection limited; if $I_{ds}$ is determined by the thin film along the channel which can be visualized as the channel resistance, the current is bulk limited \[58\].

Figure 6.12: Schematic diagram of the interface resistance and the resistance along channel.

As shown in Fig 6.12, the interface resistance and the channel resistance are represented by $R_{int}$ and $R_{ch}$, respectively. Assume the drain to source voltage $V_{ds}$ remains constant, the drain to source current of channels with respective length $L_1$ and $L_2$ are given by Equation 6.4 and 6.5.
\[ I_{ds1} = \frac{V_{ds}}{R_{ch1} + R_{int}} \]  \hspace{1cm} \text{(Equation 6.4)}

\[ I_{ds2} = \frac{V_{ds}}{R_{ch2} + R_{int}} \]  \hspace{1cm} \text{(Equation 6.5)}

On the other hand, Equation 3.5 can be rewritten as Equation 6.6,

\[ \mu_{lin} = \frac{I_{ds}}{V_{ds}} \cdot \frac{1}{W C_l (V_g - V_t)} \]  \hspace{1cm} \text{(Equation 6.6)}

Combining Equation 6.4 to 6.6, we can get the charge mobility from devices with different channels, as shown in Equation 6.7 and 6.8.

\[ \mu_{lin1} = \frac{1}{R_{ch1} + R_{int}} \cdot L_1 \cdot Q \]  \hspace{1cm} \text{(Equation 6.7)}

\[ \mu_{lin2} = \frac{1}{R_{ch2} + R_{int}} \cdot L_2 \cdot Q \]  \hspace{1cm} \text{(Equation 6.8)}

where \( Q = 1/[W \cdot C_l \cdot (V_g - V_t)] \), which is a constant, provided that the same gate voltage is taken into account.

It has been investigated that the current through p6P nanofiber is injection limited \(^{[58]}\), so it is assumed that the current through PPTPP thin film is also injection limited. Therefore, the interface resistance \( R_{int} \) is much larger than the channel resistance \( R_{ch} \), i.e. \( R_{int} >> R_{ch} \). Then Equation 6.7 and 6.8 can be changed into

\[ \mu_{lin1} = \frac{1}{R_{int}} \cdot L_1 \cdot Q \]  \hspace{1cm} \text{(Equation 6.9)}

\[ \mu_{lin2} = \frac{1}{R_{int}} \cdot L_2 \cdot Q \]  \hspace{1cm} \text{(Equation 6.10)}

If \( L_1 = 10 \mu m \) and \( L_2 = 1.5 \mu m \), then the hole mobility \( \mu_{lin1} \) should be 6 times larger than \( \mu_{lin2} \), which corresponds to values (8 times) calculated from experimental output. Moreover, as for Equation 6.7 and 6.8, if the channel resistance \( R_{ch} \) is also taken into consideration, but with much less effect compared with \( R_{int} \), then \( \mu_{lin1} \) should not be only 6 times larger than \( \mu_{lin2} \), in that \( R_{ch1} \gg R_{ch2} \). In this case, the mobility obtained from model analysis could be very near to the experimental value, namely 8 times.

The above discussion also implies that the current through PPTPP thin films is very likely to be injection limited, which can be seen from Fig 6.10 and 6.11 as well, in that large injection barrier can lead to the high threshold voltage.
Chapter 7  Optical Experiments (Emission Intensity Measurement)

Although the experiments in this chapter mainly aim at measuring light emission intensity, this emission from organic materials is due to voltage supply. Therefore, it can be also classified into the electrical property of organic materials. Under AC gate voltage, both p6P and PPTPP thin films can emit light, while p6P nanofibers seem to be unsuitable for AC gate voltage and are usually burned off perhaps due to leakage current or displacement current generated by shorting dielectric with high AC frequency.

7.1 Experimental Setup

The optical experimental setup in Fig 7.1 is based on the operating principle illustrated in Fig 4.4 (a). The drain and source electrodes are connected with two DC voltage supplies of the same type, however, of opposite polarities. The electron injecting electrode is connected with negatively biased voltage, whereas the hole injecting electrode with positively biased voltage. AC sine voltage is applied to the gate electrode by a Digimess Function Generator. But the maximum output voltage of this generator is peak-to-peak 10V, so a voltage amplifier is needed. The Falco Systems Voltage Amplifier can amplify voltage by a factor of 44. However, since there is a resistance of 50Ω in both of the function generator and the voltage amplifier, the final amplification factor of the amplifier can be regarded as 22 (See Appendix F). The oscilloscope is merely to monitor the output voltage. The sample is put in vacuum chamber and is made to be parallel with the observing window by a mechanical instrument (See Appendix G). The emitted light is collected by a ×10 optical lens and captured by the camera Infinity 1 with four second exposure. The ECO Light Source provides incandescent light which is needed to adjust the sample before observing the emitted light, and the exposure at this time should be set to a low value, normally 0.1 or 0.2 second. Otherwise the captured image would be too bright due to the light provided by the light source. When the light source is turned off after adjusting the sample in an ideal position, the exposure time should be set back to four second. It should be mentioned that it is appropriate to turn on each instrument and maintain them at lower values, and then connect the sample into the measuring circuit. Otherwise, short circuit might occur due to pulse signal and damage the sample before any measurement.
7.2 AC Gate Voltage Powered Light Emission from p6P and PPTPP thin films

When the frequency of AC voltage and its amplitude are high enough, the light emission from p6P and PPTPP thin films are easily observed. However, some parts of channel length do not emit light, which might be due to residues from lithographic process on the sample surface. Since the directly observed emission is normally too weak to be seen clearly after corresponding images being printed out or being compressed, brightness-enhanced images generated by ImageJ are also provided.

7.2.1 Light Emission at the Edge of p6P Thin Films

As discussed in Section 4.3.3, an individual electrode could function as both electron injecting electrode and hole injecting electrode. Holes injected due to negative gate voltage can meet with electrons previously injected due to positive gate voltage, thus leading to light emission. This assumption neglects the effect of channel length and implies that the semiconductor/electrode interface out of the channel region can emit light as well. To specify, 60nm p6P thin film is deposited onto a blank chip without covering the back gate, as shown in Fig 7.2 (a). The gold electrode is connected with 33V DC voltage positively. And AC voltage with frequency of 200 kHz and amplitude of 66V is applied to the back gate electrode. The interface between metal electrode and the p6P thin film emits light, while other edges of electrode without thin films remain as before. This clearly supports the assumed operating principle that one electrode can...
serve as both electron injecting electrode and hole injecting electrode. Moreover, leakage current through the dielectric could also be taken into consideration.

Fig 7.2: Illustration of light emission only from areas covered by p6P thin films (G2S5).

7.2.2 Frequency-dependent Emission Intensity

The samples G7S2 (channel length 10µm), G7S3 (5µm), G7S6 (2.5µm) and G7S7 (1.5µm) are the investigating objects in this experiment, and the other four samples in Group 7 are all short circuited. The applied AC voltage frequency are 20 kHz, 40 kHz, 80 kHz, 160kHz and 320 kHz, sequently, and \( V_d = -V_s = 30V \). The amplitude of AC voltage is approximately 50V. It should be noted that the light emitting areas of the four samples are various which might be due to residues left after the lithographic process. Therefore, the analysis of the emission intensity differences among the four samples should be done carefully, and the results might be unreliable. However, the emission intensity and the frequency relationship is much more reliable when only one sample is taken into consideration at a time, in that the residue problem can be ruled out, and the same intensity generating method, which only concerns the same emitting areas, is applied for different AC voltage frequencies. Therefore, the intensity/frequency relationship for only one sample illustrated in Fig 7.3 is reliable independently.

According to Fig 7.3, the emission intensity with arbitrary unit increases as the frequency is increased before 160 kHz, except for frequency equals to 40 kHz for samples with 1.5µm and 5µm gap. Degradation is obvious after 160 kHz for most samples except for the sample with 1.5µm gap. The amplitude values of the error bar in Fig 7.3 are provided in Table 7.1. After calculation, the error is in the range of 3.5% ~ 21%, and the average error is 6.9%.

<table>
<thead>
<tr>
<th>Gap Size (µm)</th>
<th>20 kHz</th>
<th>40 kHz</th>
<th>80 kHz</th>
<th>160 kHz</th>
<th>320 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5µm</td>
<td>23.5</td>
<td>25</td>
<td>14.5</td>
<td>27.5</td>
<td>27</td>
</tr>
<tr>
<td>2.5µm</td>
<td>30.5</td>
<td>34</td>
<td>43</td>
<td>40</td>
<td>43.5</td>
</tr>
<tr>
<td>5µm</td>
<td>24</td>
<td>34.5</td>
<td>21</td>
<td>31</td>
<td>29.5</td>
</tr>
<tr>
<td>10µm</td>
<td>23.65</td>
<td>17.15</td>
<td>35</td>
<td>22</td>
<td>18.8</td>
</tr>
</tbody>
</table>

Table 7.1: Error of measured emission intensity for various gap sizes and AC voltage frequencies.
7.2.3 Gap Size-dependent Emission Intensity

As mentioned in Section 7.2.2, the comparison among different samples might be unreliable owing to residue problem, therefore Fig 7.4 can be treated only as a reference. Among the samples with 1.5µm, 2.5µm, 5µm and 10µm gap, the sample with 2.5µm channel length seems to have largest light emission intensity at various AC voltage frequencies. This is not in accord with the conclusion made by Oyamada et al. of the investigation on DC gated OFETs with 0.8µm and 9.8µm gap samples [59]. In their experiment, the sample with 0.8µm channel length demonstrated electroluminescence about 10 times larger than that of the sample with 9.8µm channel length, and they concluded that high emission intensity is expected for the samples with much narrow gaps perhaps because the high electric field could notably modify the energy barrier near to the electron injecting electrode. However, they did not take the channel length/dielectric thickness relationship into account, which is mentioned in Section 3.2., i.e. the channel length has to be at least ten times larger that the thickness of dielectric, otherwise the lateral field from drain to source voltage could affect the field created by gate voltage. And no measurement result of samples with approximately 3µm gap was presented in their article. Besides, AC gated OFETs might not suitable to be compared with DC gated OFETs. Therefore, there seems to be no conflict.

In order to make the experiment relevant to gap size dependence more reliable, the residue problem should firstly be overcome in future to make sure most of the channels can emit light.
7.2.4 Emission Difference between p6P and PPTPP Thin Films

The light emission from 32nm PPTPP thin film is significantly weak and only limited to two or three channels, which might be owing to the already-damage from high voltage and frequency, as shown in Fig 7.5 (a). The corresponding brightness-enhanced image is illustrated in Fig 7.5 (c). The damage area is marked by a circle in these two figures. In contrast to PPTPP, the light emission from p6P thin film seems to be more uniform, though areas of unlit parts exist, as illustrated in Fig 7.5 (b) and brightness-enhanced image Fig 7.5 (d). Since no emission spectra of these devices are recorded, it is not appropriate to make a quick judgment whether they are normal emission due to hole-electron recombination from PPTPP or p6P. However, comparing the two images in the lower panel, it is easy to distinguish the green light from PPTPP thin film and the blue light from p6P thin film, which is in accord with the previous observed light emission. \[14\][60].

![Fig 7.4: Illustration of intensity/gap size relationship for different AC voltage frequencies.](image-url)
Chapter 7  Optical Experiments (Emission Intensity Measurement)

7.2.5 Measurement Circumstances Dependence
The above presented light emissions are all observed from samples under vacuum condition (approximately $5 \times 10^{-3}$ Pa). Despite of the residue problem, light emission is noticeable even at a lower AC voltage frequency, for instance 20 kHz, when the amplitude of AC voltage is not too low, for example larger than 50V. On the other hand, only two samples of Group 1 (nine samples with 1.5µm gap, see Appendix E) emit relatively continuous light in ambient air. And the so-called continuous light vanishes almost immediately. Its corresponding operating parameters are $V_d = -V_s = 35$V, $V_g = 66$V and $f = 200$ kHz. Besides, only blinks are observed from other samples in Group 1 under ambient air, even the amplitude of AC voltage is tuned to 110V. Moreover, if the frequency and amplitude of AC voltage is too high, the sample is easily damaged which can be indicated by white sparks. The blinking and damaging process of samples in ambient air are hard to be captured by optical camera, due to long exposure time of the camera and short time of sample blink.

Since the carrier recombination involves both holes and electrons, even oxygen and water in air could barely influence p-channel transistors, electrons might be captured, leading to unnoticeable emission or no emission. The charge density of holes could be increased due to gradual fewer electrons, which destroys electrodes.

7.2.6 Sample Degradation and Damage
As discussed in Section 4.3.3, higher frequency can result in more intensive light emission due to
increased number of electrons and holes involving in the recombination process. On the other hand, if the high AC voltage frequency can make the electrons inject from metal electrode rapidly enough before holes reaching the other end of channel or visa versa, then it makes sense as well that higher frequency induces brighter emission light. However, according to Fig 7.3, the decrease of the emission intensity of most curves is noticeable, except for the sample with 1.5 µm channel length. It should be mentioned that the intensity decrease does not necessarily occur only after 160 kHz. The AC voltage frequency of 200 kHz is also tested for other samples, and the resulting emission intensity seems larger than that generated from 160 kHz. Therefore, the trend indicated by Fig 7.3 only provides a general idea that degradation could happen if the frequency of AC voltage is too high.

Moreover, the degradation owing to high frequency seems to be irreversible. After the series of frequencies, from 20 kHz to 320 kHz, is applied to the sample with 2.5 µm gap, a second series of measurement is carried out after two minutes, also keeping \( V_d = -V_s = 30 \text{V} \) and the amplitude of \( V_g \) is 50V. The obtained intensity is much lower than that obtained for the first series measurement, as provided in Table 7.2. The same degradation phenomenon is observed for the sample with 1.5 µm as well.

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>Series 1</th>
<th>Series 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>571.5</td>
<td>191</td>
</tr>
<tr>
<td>40</td>
<td>70.5</td>
<td>241.5</td>
</tr>
<tr>
<td>80</td>
<td>992.5</td>
<td>416</td>
</tr>
<tr>
<td>160</td>
<td>1123.5</td>
<td>544.5</td>
</tr>
<tr>
<td>320</td>
<td>1046</td>
<td>586.5</td>
</tr>
</tbody>
</table>

Table 7.2: Comparison of emission intensity obtained from two series of measurement. The series 2 measurement is taken two minutes after the series 1 measurement has been finished.

The intensity decrease from Series 1 and Series 2 measurement also implies that the degradation takes place dramatically quickly, in that only two-minute time interval exists between the two measurements. In contrast, the degradation obtained in the electrical measurement discussed in Chapter 6 happens much slower, which could be counted by day. In this sense, the degradation owing to high frequency and amplitude of AC gate voltage could be called damage.

However, the real damage is much severer than the above mentioned degradation-like damage. As shown in Fig 7.6 (a), the sample is completely destroyed after being applied an AC gate voltage with frequency 600 kHz and amplitude 88 V, while keeping \( V_d = -V_s = 30 \text{V} \). Before the damage, the parameters are kept at \( f = 200 \text{kHz} \), amplitude of \( V_g = 88 \text{V} \) and \( V_d = -V_s = 30 \text{V} \). The damage takes place suddenly when the frequency is tuned from 200 kHz to 600 kHz, and the damage is so severe that the p6P thin film is burned off, which can be distinguished from the background color between Fig (a) and (b). An AFM image of the G2S8 damage with a scanning area 10µm × 10µm is shown in Fig 7.6 (c), together with the corresponding profile of damaged Au electrode in (d). It can be seen that the damaged parts are definitely not residues of organic materials, but defects of electrodes after being destroyed. Several SEM images are provided in Appendix H.

Fig 7.6 (b) illustrates another destroyed sample G7S6, which is under the parameters at \( f = 320 \text{kHz} \), amplitude of \( V_g = 50 \text{V} \) and \( V_d = -V_s = 30 \text{V} \). The damage of this sample is much less dramatic than that in (a), and the p6P thin film appears intact. It also should be noted that most of the damages are happened to the negatively biased metal electrode, namely the electron injecting electrode.
Since the dielectric breakdown strength of SiO₂ is 10 MV/cm, the 200nm SiO₂ is likely to tolerate external voltage of around 200V. For the I-V measurement in Chapter 6, the samples are normally capable of tolerating voltage of 130V, including the drain to source voltage V_{ds} and DC gate voltage V_{g}, and even degradation could show up when V_{g} is relatively high, but if the sample is disconnected with the circuit for some time, its performance is restored. In contrast, for the light emission measurement, the samples can be destroyed completely with the same total voltage, approximately 130V. A possible explanation is that high frequency AC gate voltage might lead to displacement current, which contributes to this damage or even the rapid irreversible degradation.

7.2.7 Light Emission from Individual Electrode
As discussed in Section 4.3.3, considering the charge carriers of both polarities injected or tunneled from metal electrode, light emission might be observed as well without taking the channel length into account. For the relevant experiment, one metal electrode is connected with negatively biased DC voltage, i.e. -30V, and an AC voltage with frequency 200 kHz and amplitude 77V is applied to the gate electrode, this individual electrode can also emit blue light as expected, as shown in Fig 7.7. Moreover, if the negatively biased DC voltage is substituted with a positive
voltage, light emission can be observed as well, but weaker due to degradation.

![Image](a) ![Image](b) ![Image](c)

**Fig 7.7:** Illustration of individual emitting electrode of sample G2S7 without connecting the other electrode into circuit.

### 7.3 Light Emission Investigation of p6P Nanofibers

Fig 7.8 shows a sample with 5nm p6P nanofibers before light emission intensity measurement, and the corresponding fluorescence image has already been presented in Fig 5.4 (b). The experiment is also taken under vacuum, $5 \times 10^{-3}$ Pa. The drain and source voltages are respectively kept at $\pm 30$, and the frequency of AC gate voltage is increase from 2 kHz, 20 kHz, 40 kHz, 80 kHz and 160 kHz. The amplitude of AC voltage is no more than 55V. Five images corresponding to the series of frequencies are taken, but no light emission is obtained. After the measurement, the metal electrode connected with negatively biased DC voltage is short-circuiting. The most unsatisfactory result is that all the p6P nanofibers are burned off, perhaps due to short circuit of electrode.

It is strange that light emission is not obtained from nanofibers during the whole process. Although it might be argued that the p6P nanofibers have been burned off owing to short circuit of electrode, and it is hard to determine when the short circuit occurs, so obviously no emission can be observed. However, the voltage parameters for the second image are $V_d = -V_s = 30V$, $V_g = 50V$ and $f = 20$ kHz, the sample is very unlikely to be shorted under such parameters. And more disordered p6P thin films have already emitted weak blue light under these conditions, but no emitting light is gained from crystalline nanofibers which should facilitate the electron injection at the semiconductor/electrode interface.

Nevertheless, it should not make a quick conclusion based on only one sample that nanofibers are not suitable for AC gated operating manner. More experiment should be carried out to determine the optimized parameters for nanofibers.
Fig 7.8: Illustration of 5nm p6P nanofibers on a chip with 1.5µm channel length, corresponding to Fig 5.4 (b).
Chapter 8 Conclusion and Outlook

Para-hexaphenylene (p6P) and 2,5-bis (4-biphenylyl) thiophene (PPTPP) are conjugated molecules which can act as building blocks of organic nanofibers and thin films. Such organic materials could possess high charge carrier mobility due to edge-to-face or face-to-face \( \pi \)-orbital-stacking between neighboring molecules. Muscovite mica with polarized surface can be served as growing substrate of p6P and PPTPP nanofibers, but it is a significant challenge to transfer these nanofibers onto other device substrates owing to their low solubility and contamination-vulnerability. In contrast, p6P and PPTPP thin films can be deposited directly onto device substrates, but resulting in amorphous form compared with corresponding crystalline nanofibers.

Organic field-effect transistor (OFET) can be utilized as the platform to elucidate the charge carrier transporting mechanism of organic nanofibers and thin films. Three configurations of OFET (BC/BG, TC/BG and BC/TG) can be classified based on the relative positions of three electrodes (source, drain and gate) dielectric and active organic layer. According to the polarity of major charge carriers in the transporting channel, OFET can be divided into unipolar (p-channel and n-channel) and ambipolar devices. The active organic layer is not necessarily p-type or n-type. Instead, factors such as type of metal electrodes, the dielectric layer and the ambient air, determine the polarity of the transporting channel.

Electrical and optical functions can be integrated into OFET, leading to the realization of organic light-emitting field-effect transistor (OLEFET). Light emission can be observed from DC gated OLEFET with unipolar carrier transporting channel, but the light emission only occurs in the vicinity of one metal electrode, which could be due to lopsided injection of holes and electrons in unipolar channel. In contrast, holes and electrons can be injected from respective metal electrodes simultaneously with similar mobilities in ambipolar OLEFET, thus moving the emission zone toward the center of transporting channel, resulting in more intensive light emission, which can be attributed to the efficient recombination of holes and electrons. Ambipolar OLEFET can also be driven by AC gate voltage, but the relative emission mechanism is still open to debate and investigate.

In the electrical experiment part of this project, DC voltage is connected with the back gate of OFET devices with BC/BG configuration. The p6P and PPTPP thin films are chosen to be the active organic layer. The hole mobilities calculated for p6P and PPTPP thin films are approximately three or four order magnitudes less than that expected, which could be owing to the ambient air measurement circumstance. No measurement investigating electron mobility of p6P and PPTPP thin films is carried out. It is interesting that the calculated hole mobilities seem to depend on channel length of the devices, which could be explained as the result of injection-limited drain to source current of the p6P and PPTPP thin films. Besides, both of the films exhibit high threshold voltage of holes, -40V and -20V, respectively, which also implies the non-ohmic contact between metal electrode and organic layer.

In the light emission experiment part, AC gate voltage is utilized to drive the BC/BG OFET devices. If the frequency and amplitude of AC gate voltage are adequately high, light emission can be obtained not only from the carrier transporting channel, but also from other electrode/organic semiconductor interfaces, both for p6P and PPTPP thin films. Besides, light emission can be observed as well from individual metal electrode, while completely disconnecting the other
This could be explained by a model in which individual electrode can function as both hole and electron injecting electrode under the drive of AC gate voltage. The AC frequency dependence and channel length dependence of the emission intensity are also investigated in this experiment part, together with sample degradation and damage study. The OFET devices can be degraded under AC gate voltage much faster than under DC gate voltage. Moreover, p6P nanofibers transferred onto OFET device by a novel method are burned off under AC gate voltage, which could be due to previous device short circuit or the unsuitability of nanofibers for the drive of AC gate voltage.

Although field-effect characteristics of OFET device based on organic thin films are obtained in this project, and the organic thin films can also be light up by AC gate voltage, the investigation results of corresponding nanofibers is not as expected, partly because of limiting experiment time near the end of this semester, partly because of the difficulty in transferring nanofibers from mica to transistor substrates. It is expected that a reliable nanofiber-transferring method can be realized in future work, which could notably improve experimental efficiency and outcome relevant to organic nanofibers. Besides, a few ideas and possible investigation methods are listed as follows:

- The p6P and PPTPP crystals could be modified into new derivatives in which the π-orbital overlaps are promoted, namely from edge-to-face to face-to-face alignment manner among neighboring molecules.

- Qualified SiO2 dielectric is very importance to the electrical experiment involving in high DC or AC gate voltage. Many short circuits occur during the experiment of this project, which could be due to the thin layer (200nm) of dielectric possessing excessive pinhole. Therefore, the quality of SiO2 dielectric should be guaranteed in future experiment and thicker dielectric could be tested, for instance 300nm in thickness.

- New OFET device configuration could be utilized, for example, using asymmetric metal electrodes which facilitate the injection of both electrons and holes, or using the BC/TG device structure to amplifier the effect of gate.

- The mechanism of AC gated OLEFET is not fully understood, which could be simulated based on a model consisting of individual-electrode injections and hole-electron recombination within transporting channel.
Appendix A: Illustration of Several PPTPP molecule orbitals

Fig A.1: Illustration of HOMO (a) and HOMO-1 (b) of PPTPP oligomer.

Fig A.2: Illustration of LUMO (a) and LUMO+1 (b) of PPTPP oligomer.
Appendix B: Derivations of Charge Mobility

The drift current density of organic semiconductors can be determined by Equation B.1, in which both of holes and electrons are taken into consideration\(^\text{[61]}\).

\[
J = \sigma \cdot E = q \cdot \left( \mu_e N_e + \mu_h N_h \right) \cdot E \quad \text{(Equation B.1)}
\]

Where \( \sigma \) is given by

\[
\sigma = \frac{1}{\rho} = q \cdot \left( \mu_e N_e + \mu_h N_h \right) \quad \text{(Equation B.2)}
\]

\( \sigma \) and \( \rho \) are the conductivity and resistivity, respectively; \( q \) is the elementary charge; \( \mu_e \) and \( \mu_h \) are respectively the electrons mobility and the holes mobility; \( N_e \) and \( N_h \) are respectively the electrons concentration and holes concentration.

Since p-type channel is much more common in practice to date, it is assumed here that \( N_h \gg N_e \). Therefore

\[
\rho = \frac{1}{q \cdot \left( \mu_e N_e + \mu_h N_h \right)} \approx \frac{1}{q \cdot \mu_h N_h} \quad \text{(Equation B.3)}
\]

And

\[
J = \sigma \cdot E = \frac{1}{\rho} \cdot E = q \cdot \mu_h N_h \cdot E \quad \text{(Equation B.4)}
\]

In fact, the basic current density is given by the following equations

\[
J_e = q \cdot \mu_e N_e E + qD_e \nabla N_e \quad \text{(Equation B.5)}
\]

\[
J_h = q \cdot \mu_h N_h E - qD_h \nabla N_h \quad \text{(Equation B.6)}
\]

\[
J_{\text{total}} = J_e + J_h \quad \text{(Equation B.7)}
\]

The second terms on right-hand side of Equation B.5 and Equation B.6 are the diffusion components due to the carrier concentration gradient within the channel, which are neglected in above derivations for simplicity.

To further simplify the following discussion, Equation B.4 is turned to

\[
J = q \cdot \mu \cdot N \cdot E \quad \text{(Equation B.8)}
\]

Again, neglect the carrier concentration gradient in the channel, the total mobile charge carriers are assumed to occupy a rectangular object with height \( H \), and the length and width are the channel length \( L \) and channel width \( W \), respectively. Then, the mobile charge \( Q_i \) induced by gate voltage \( V_g \) per unit area is

\[
Q_i = \frac{Q}{W \cdot L} \quad \text{(Equation B.9)}
\]

The mobile charge \( Q_v \) per unit volume is

\[
Q_v = \frac{Q}{W \cdot L \cdot H} \quad \text{(Equation B.10)}
\]
where \( Q \) is the total mobile charge.

On the other hand, the mobile charge \( Q_v \) can be defined as

\[
Q_v = q \cdot N
\]  
(Equation B.11)

Combine the above four equations from Equation B.8 to Equation B.11, we obtain

\[
J = q \cdot \mu \cdot N \cdot E = Q_v \cdot \mu \cdot E = \frac{Q_i}{H} \cdot \mu \cdot E = \frac{W \cdot Q_i}{W \cdot H} \cdot \mu \cdot E
\]  
(Equation B.12)

Finally, the drain to source current can be determined by the following equation

\[
I_{ds} = J \cdot W \cdot H = W \cdot Q_i \cdot \mu \cdot E
\]  
(Equation B.13)

And, the definition of mobile charge per unit area has already been represented by Equation 3.4 in Section 3.2

\[
Q_i = C_i \cdot (V_g - V_t)
\]
Appendix C: Description of Chips Fabricating Processes in Cleanroom

- **HMDS treatment**
  A monolayer of Hexamethyldisilane (HMDS) is deposited onto the starting wafer in vapor form in HMDS treatment oven. The HMDS monolayer acts as the adhesion promoter, one end binding to the SiO₂ surface and another end binding to the following deposited resist. This process takes about 30 min, and the wafer should be cooled itself for 10 min before depositing resist. It is appropriate to check the liquid HMDS status before carry out this treatment. The liquid HMDS in good condition is expected to be transparent. If it turns to yellow, it might be due to expiration or there might be only residua in the HMDS bottle. If the undesirable liquid HMDS condition is noticed unfortunately after the HMDS treatment, the thickness of the subsequently spun photo resist should be checked under profilometer.

- **Spin on photo resist**
  An image reversal photoresist AZ 5214 is then spin-coated onto the wafer by EBS11 spinner. First a rotation of 500 rpm for 5 sec is applied to spread out the resist generally, which is followed by a much faster rotation of 4000 rpm for 30 sec to obtain a uniform resist layer of 1.5 μm. Various values of slow rotation can be chosen in order to try to get a more uniform film, but the fast rotation should not be different if the same thickness resist film is desired. It is also recommended to check the status of photo resist before spinning. If there is only residuum or small amount of resist in the photo resist bottle, it is strongly suggested to change the whole bottle. Otherwise, there will be more bubble than expected during the spinning process, leading to very unsatisfactory results on some spots of the wafer. If a brand new bottle of photo resist is ready before spinning, it is also recommended to waste a small amount of resist spinning on test wafer, in that bubbles are prone to show up from a new bottle of resist.

- **Pre-bake**
  After resist spinning, the wafer is prebaked at once at 100°C for 60 sec on Prazitherm Pz 2860SR hot plate. This process can remove the remaining solvent from the resist and it can also increase the bonding between HMDS and the wafer as well as the resist, respectively. Moreover, the stress due to spinning process can be relived to some extent.

- **UV negative exposure**
  Leave the wafer for about 1 min after pre-bake. And then the wafer is exposed to UV light for 1.7 sec in soft contact mode by KS MA 150 mask aligner, as the step (1) and (2) showed in Fig C.1.
Like before, it is always a good idea to check vital components before real experiment. In this step, the status of mask should be examined under optical microscope. If there is much more noticeable dust than normal on the mask due to long time usage, it is better to clean the mask. Otherwise, the expected elaborate electrode channels are much likely to be damaged.

- **Reversal bake**
  The wafer is then immediately reversal baked on Prazitherm Pz 2860SR hot plate at 130°C for 120 sec. This process makes the previous exposed soluble areas insoluble in the developer by activating the cross-linking agent in the resist, as the step (3) showed in Fig C.1.

- **Flood exposure**
  Again, leave the wafer for about 1 min before the flood exposure for 30 sec. This process makes the previous unexposed areas soluble in the developer [see step (4) and (5)]. The inert area is light insensitive due to reversal bake. If the flood exposure is not applied, then much of the undesired resist remain even after development process. In that case, almost the entire resist with metal on top will be removed in the lift off process, leading to extremely disappointing results.

- **Development**
  The wafer is then developed in AZ 351 B developer at 22°C for 1 min followed by 2 min water rinse (bubble rinse for the latter half minute). After that, it is dried using a spin dryer. An undercut profile is finally achieved [see step (6)]. The quality of AZ 351 B developer is very sensitive to temperature. It is better to maintain the temperature within the range of 21.8 to 22.2°C.

- **Metal deposition**
  A titanium layer with a thickness of 2nm followed by 30nm of gold layer is deposited on the wafer.
by the e-beam evaporator of Cryofox 600 thin film deposition system. The rate is set to be 1/2 Å per sec for Ti/Au, respectively.

- **Lift-off**

Finally, the wafer is placed in an ultra-sonic acetone bath. At the first 3 min, no ultra-sonic agitation is applied. And then, ultra-sonic agitation is given gradually so as to remove the remaining resist with metal on top. It takes about 5 min totally for this process. 2 min water rinse is then required (bubble rinse for the last minute). After that, it is dried by a spin dryer.

The above processes are intended to fabricate metal electrodes. An ideal electrode channel structure with 25 µm channel length is illustrated in Fig C.2 (a). The results of other electrodes with 2.5 µm, 5 µm, 10 µm and 50 µm are also satisfactory. However, a large amount of black residue tend to lie between source and drain electrodes for the 1.5 µm channel length due to unknown reasons, as shown in Fig C.2 (b). In this case, after the whole chips fabrication processes, the wafer could be treated with O₂ plasma for one or two treatment cycles, each cycle lasting 3.5 minutes. The treatment power should be under 200 W ensuring the structures on the wafer are not damaged. However, the black residue for 1.5 µm channel length is not found on some wafers. It is also strongly recommended to treat the wafer with O₂ plasma before dicing.

![Fig C.2: (a): Metal electrodes with 25 µm channel length. (b) Illustration of black residues for 1.5 µm channel length.](image)

The back gate pads fabrication process, which is similar to making electrodes, is briefly introduced as follows:

- **HMDS treatment; Spin on photo resist; Pre-bake**
- **UV negative exposure**

In this step, apart from substituting the electrodes mask with back gate pads mask, it is of vital important to ensure the back gate pad to be moved to the middle of source and drain pads after the normal alignment has been done, in that in this project the back gate pads mask is not designed for the electrodes mask. It is certainly better to make a new back gate pads mask based on the electrodes location of the electrodes mask. However, considering the cost and complexity to make a new mask and the simplicity to move the current mask laterally a little bit without rotation after alignment, it is not suggested to make a new one.

- **Reversal bake; Flood exposure; Development**
- **Etch out back gate windows with buffered hydrofluoride acid (bHF)**
After development, the wafer is immersed in bHF, which only attacks SiO₂ but not Si, for 3 min 20sec in order to etch out the back gate windows thoroughly. The buffer HF consists of HF acid and ammonium fluoride, which makes the etching rate unchanged at 75 nm per min. Water rinse for 5 min is required subsequently.

- **Metal deposition**
  A titanium layer with a thickness of 10nm followed by 50nm of gold layer is deposited on the wafer. The rate is set to be 1/2 Å per sec for Ti/Au, respectively. It should be highlighted that the metal deposition for the back gate pads must be carried out immediately after the above bHF acid step, in an attempt to avoid the oxidation of the exposed Si after its top SiO₂ is etched out.

- **Lift-off**
  Since the Ti/Au layer in this case is considerably thicker than that in the electrode-fabrication process, it is much more difficult to lift off the metal at undesired areas. Therefore, there is no restricted treatment time in this step, as long as expected metal structures have not become clear.
# Appendix D: Optimized Parameters for Wire Bonding Machine

<table>
<thead>
<tr>
<th>Loop</th>
<th>SEARCH</th>
<th>FORCE</th>
<th>TIME</th>
<th>POWER</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.9</td>
<td>2.7</td>
<td>3.9</td>
<td>0.2</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Appendix E: Summary of Sample Groups

<table>
<thead>
<tr>
<th>Group</th>
<th>Sample quantity</th>
<th>Gap sizes (sequence number: gap size)</th>
<th>Active organic materials</th>
<th>Additional description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group 1</td>
<td>9</td>
<td>1~9: 1.5μm</td>
<td>60nm p6P thin films</td>
<td>☆</td>
</tr>
<tr>
<td>Group 2</td>
<td>10</td>
<td>1<del>6: 1.5μm 7</del>10: 2.5μm</td>
<td>60nm p6P thin films</td>
<td>□;☆</td>
</tr>
<tr>
<td>Group 3</td>
<td>7</td>
<td>1<del>2: 1.5μm 3</del>7: 2.5μm</td>
<td>No materials</td>
<td>☆; Sample 1: test whether SiO$_2$ can emit light due to AC gated Voltage.</td>
</tr>
<tr>
<td>Group 4</td>
<td>14</td>
<td>1<del>3: 5μm 4: 1.5μm 5</del>8: 2.5μm 9<del>11: 10μm 12</del>14: 25μm</td>
<td>For 5 nm p6P nanofibers</td>
<td>☆; Almost no satisfactory transferring results except for Sample 6 and 7.</td>
</tr>
<tr>
<td>Group 5</td>
<td>10</td>
<td>1<del>4: 5μm 5</del>7: 10μm 8~10: 25μm</td>
<td>24nm p6P thin films</td>
<td>□</td>
</tr>
<tr>
<td>Group 6</td>
<td>10</td>
<td>1<del>4: 1.5μm 5</del>7: 5μm 8~9: 10μm 10: 25μm</td>
<td>32nm p6P thin films</td>
<td>□;☆</td>
</tr>
<tr>
<td>Group 7</td>
<td>8</td>
<td>1<del>2: 10μm 3</del>4: 5μm 5<del>6: 2.5μm 7</del>8: 1.5μm</td>
<td>60nm p6P thin films</td>
<td>☆</td>
</tr>
<tr>
<td>Group 8</td>
<td>6</td>
<td>1<del>2: 1.5μm 3</del>4: 2.5μm 5~6: 5μm</td>
<td>60nm p6P thin films</td>
<td>☆; Chips are treated by OTS before depositing thin films</td>
</tr>
</tbody>
</table>

□ indicates that the corresponding group is for electrical measurement;
☆ indicates that the corresponding group is for light emission measurement.
Appendix F: Calculation of Applied AC Gate Voltage

![Diagram](image)

Fig F.1: Illustration of the relationship between output voltage of voltage amplifier and the original voltage supplied by the function generator.

$V_{pp}$ is the voltage supplied and displayed by the Function Generator, which has an internal resistance 50Ω. The voltage amplifier also has an internal resistance 50Ω. Therefore, the voltage $V_{in}$ is the half of that supplied by the Function Generator due to a voltage distribution, namely,

$$V_{in} = \frac{V_{pp}}{2} = V_p$$

$V_{in}$ is multiplied by the amplification factor 50, and $V_{out}$ in then obtain, which is the amplitude of AC gate voltage after amplifying

$$V_{out} = 50 \cdot V_{in} = 25 \cdot V_{pp}$$

For instance, if the peak-to-peak voltage supplied by the Function Generator is 3.0V, then the voltage distributed at the output end is 1.5V, which is then multiplied by the amplification factor 50 and the final output voltage is 75V (so the amplification factor can be regarded as 25 (75/3.0) with respect to the original input 3.0V). And then the amplitude of the output AC voltage is 75V.

But practically, the amplification factor is no more than 44 perhaps due to calibration problem (so the amplification factor can be regarded as 22).

From above discussion, it can be concluded that if the Function Generator provides 3.0V, then the amplitude of the output voltage from the amplifier is 66V. If the Function Generator provides 2.3V, then the amplitude of the output voltage from the amplifier is approximately 50V.
Appendix G: Sample Holder

Fig G.1: Photograph images of sample holder.
Appendix H: Sample Damage after Light Emission Measurement

Fig H.1: SEM image of a portion of the damaging passage.

Fig H.2: SEM image of one of the damaging origins and resulting damaging passage, with magnification of 1,500.
The electrode damage of the sample G2S8 is illustrated in several SEM images, from Fig H.1 to Fig H.3. As shown in Fig H.1 and its inset, the edge of the damaging passage is irregular and no residue organic material could be possibly observed. Fig H.2 illustrates the origin of the damage, which is located in the lower left part of this image. This origin leads the damaging passage even to reach the other side of metal electrode, as the part marked by red circle show. Fig H.3 provides a closer look of the damaging origin, indicating the 200nm SiO2 dielectric might be completely pierced.
References


