Organic light-emitting transistors with optimized gate dielectric

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JUNE, 2013

ABSTRACT

Organic materials have been developed as promising candidates in a variety of electronic and optoelectronic applications due to its semiconducting properties, synthesis, low temperature processing and plastic film compatibility. Hence, the organic light emitting transistor (OLET) has attracted considerable interest in realizing large-area optoelectronic devices and made tremendously progress in recent years. In order to further improve the device performance, one possibility is to optimize the gate dielectric material. Typically, silicon dioxide (SiO2) works as gate dielectric. However, SiO2 traps electrons at the semiconductor/dielectrics interface, which can prevent charge carriers transport. Therefore, the focus of this project is to look into the performance of OLETs with optimized gate dielectrics and investigate the improvement compared with conventional OLETs.

The optimized gate dielectric used in this project is poly(methyl methacrylate) (PMMA), which is a promising polymer material. The device is developed with bottom contact/bottom gate (BC/BG) and top contact/bottom gate (TC/BG) configuration. Taking BC/BG configuration as an example, in an OLET, silicon substrate PPTTPP thin film acting as organic semiconductor is connect to gold (Au) source and drain electrodes, which is positioned on top of PMMA layer on Au bottom layer. Aluminum (Al) also be investigated as source and drain electrode. Then a suitable microfabrication recipe is introduced, which involves the fabrication recipe of stencil. The fabrication process is realized in clean room and optical lab, followed by the electrical and optical measurements to characterize the devices.

The devices show good electrical performance and p-channel characteristics. The study is based on different gate dielectric, configuration, S/D electrode material and channel length. The transistor based on TC/BG configuration using PMMA as gate dielectric Au as electrode and 25μm as channel length exhibits the best performance of mobility up to $9.69*10^{-3} cm^2 vV^{-1} s^{-1}$, low leakage current on the order of 10^{-9}A.

All the related experimental process and results are disserted in this thesis. And a summary and outlook are also given in the last chapter.

PREFACE

The master thesis regarding organic light-emitting transistors with optimized gate dielectric is based on my theoretical study and experimental research carried out from September of 2012 to June of 2013 in NanoSYD, Mads Clausen Institute at University of Southern Denmark. The project counts 40 ECTS and is supervised by Associate Professor Jakob Kjelstrup-Hansen and co-supervised by Per B. W. Jensen, a PhD student in the NanoSYD group.

During this project, I have received generous support from many people, which I really appreciate. First, I would like to express my gratitude to my supervisor Jakob Kjelstrup-Hansen. He offered tremendous support in every aspect of the project, including theoretical and experimental part. I also would like to thank Per B. W. Jensen. He helped me a lot with operating the PPTTPP chamber, electrical and optical characterization, preparing substrates etc. Moreover, Luciana Tavares helped me with fabricating stencils. Jacek Fiutowski gave some guidances about operating PPTTPP chamber. Morten Madsen gave me the introduction of operating Edwards deposition machine. Arkadiusz Jaroslaw Goszczak gave me advices of AFM operation. I also want to thank Kasper Thilsing-Hansen, the technical manager. He taught me how to operate AFM and Ellipsometer and gave me great suggestions on various instruments in cleanroom, especially deposition procedure. Thanks are also given to other fellows in NanoSYD group and all my classmates.

ABBREVIATIONS

AC voltage	Alternating-Current voltage
AFM	Atomic Force Microscope
BCB	Benzocyclohutene
BC/BG	Bottom Contact/Bottom Gate
BC/TG	Bottom Contact/Top Gate
CaO	Calcium oxide
DC voltage	Direct-Current voltage
HMDS	Hexamethyldisilane
HOMO	Highest Occupied Molecule Orbital
IPA	isopropanol
KOH	potassium hydroxide
LUMO	Lowest Unoccupied Molecule Orbital
OFET	Organic Field-Effect Transistor
OLED	Organic Light-Emitting Diode
OLET	Organic Light-Emitting Transistor
PE	Polyethylene
PEN	polyethylenenaphthalate
PMMA	Poly(methyl methacrylate)
PI	Polyimide
PS	Polystyrene
PVP	poly 4-vinyl phenol
TC/BG	Top Contact/ Bottom Gate
SAM	Self-Assembled Monolayers
SiO2	silicon dioxide

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CHAPTER 1 INTRODUCTION

With the rapid developing of semiconducting industry, organic semiconductor exhibits its appealing features compared to the conventional semiconductor materials. To date organic materials are already used in commercial products for example in OLED displays in mobile phones, energy technology like solar cells, field-effect transistors investigating in this project and other expected future applications. The use of organic materials is attractive to build electronics for its properties of low cost, mechanical flexibility, straight-forward processing method, chemical synthesis etc.

In this project, I works with such materials to fabricate organic light-emitting transistors (OLETs) and I am looking for possible aspects to improve the device performance especially energy efficiency. For an OLET, the organic semiconductor layer is separated from gate electrode by a gate dielectric layer, source and drain electrodes are in contact with the semiconducting material. By applying a suitable voltage to the gate, the conductance of the organic semiconductor can be modulated and under certain conditions, holes and electrons can meet to recombine and emit light.

For dielectrics, silicon dioxide (SiO2) is typically used. With thermally grown SiO2 gate insulators combined with organic semiconductors, it provides conventional base to obtain the OFET device, as silicon dioxide is readily available from Si technology. However, the problem of charge trapping by the gate dielectric material indicates its limitation, which will prevent the transport through the transistor. Polymer dielectrics are a promising alternative material to improve the device performance via reducing charge trapping and thereby resulting in a higher energy efficiency device. Polymethyl methacrylate (PMMA) is a polymeric material with thermal and mechanical stability, high resistivity, suitable dielectric constant, which leading to PMMA as a promising material as a dielectric layer.

Hence, this project focuses on developing and characterizing OLETs with such optimized gate dielectrics and investigating its performance with PPTTPP as organic semiconductor. Configuration, channel length and electrode material are also investigated in the this project.

Chapter 2 introduces the operation principle, configurations, current – voltage characteristics, classification of organic field-effect transistors (OFETs). Unipolar and ambipolar OFET also been discussed in this chapter, which is decided by the charge transport in the channel. Furthermore, the organic light-emitting field-effect transistor (OLET) as an important potential application is presented with its theoretical foundation of the experiments, including DC voltage gated and AC voltage gated operation.

Chapter 3 gives a general introduction of the dielectric materials, including the working principle, the conventional material silicon dioxide, and possible solution to improve the property of silicon dioxide. By comparing the advantage and disadvantage of potential materials, the polymer dielectrics is the most interesting material to be used. And Polymethyl

methacrylate (PMMA), which is one of the polymer materials, is mainly been investigated in this project, which is expected to improve the device performance via reduced charge trapping and thereby result in higher energy efficiency.

Chapter 4 aims at experiment details of fabrication process of the OFET device. investigate the breakdown voltage of PMMA dielectric layer, design and fabrication of stencil are also included. The OFET devices are fabricated based on different configuration (TC/BG and BC/TG), source and drain electrode (gold and aluminum) and channel length. And the short circuit measurement is also involved acting as a prerequisite measurement of OFET.

Chapter 5 presents and summarizes the results of electrical experiments for OFETs. The outcome focus on transfer characteristics (drain current versus gate voltage at constant source-drain voltage) and output characteristics (drain current versus source-drain voltage at constant gate voltage), and then extract the mobility and threshold voltage. This chapter highlights the field-effect properties by the configuration and channel length on the performance of OFET device.

Chapters 6 summarize the outcome of electrical experiments for OFETs and give some outlook of future works.

CHAPTER 2 ORGANIC FIELD-EFFECT TRANSISTOR (OFET)

In this chapter, OFET is introduced by illustration its operation principle, configurations, current – voltage characteristics, classification based on charge carriers transport channels. Thus, the derivation of charge mobility and threshold voltage and critical factor determining unipolar and ambipolar types can be inferred. Furthermore, as a crucial potential application, the organic light-emitting transistor (OLET) is presented. The theoretical foundation of electrical measurement for OFET and optical measurement for OLET is also presented, including the two different operation methods are discussed, that is, DC gate voltage operation, and AC gate voltage operation.

2.1 Working principle

Organic field-effect transistor (OFET) is based on field-effect transistor and using an organic material in its channel. An OFET device requires the following components: electrodes, organic semiconducting layer, and dielectric layer. Organic Semiconductor, for example, P6P or PPTTPP layer is governed by its energy of the molecular orbitals and mobility of the majority charge carries. Vacuum evaporation and transfer technique can both be used to deposition. Dielectric layer can be both organic and inorganic material and silicon dioxide (SiO_2) is the most common material used. However, due to charges trapped in SiO_2 layer, this project is expected to intrigue different material than can improve the device performance. The possible candidates can be polymethyl methacrylate (PMMA), polystyrene (PS) etc. The three terminals (source, drain and gate electrode) require suitable work function material to match the energy level of organic semiconductor so that decreasing the charge barrier. The function of source and drain electrodes is emitting and receiving charge carriers from the channel. Gate electrode modulates the charges in the channel. Applying high gate voltage leads to high current flow in the channel. Typically, high work function material is used for p-channel OFETs.

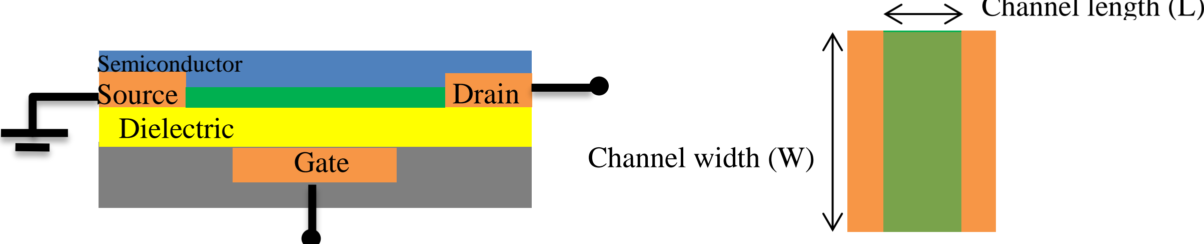


Figure 2.1. Schematic configuration of an OFET based on BC/BG configuration with cross-section view (left) and top view (right)

Figure 2.1 shows the cross-section and top view of the device, the distance between source

and drain is channel length (L) and the other direction along the channel is channel width (W), which forms an area at the semiconductor- dielectric interface allowing charges (electrons or holes) flows between source and drain electrode.

An OFET device works by applying voltage on its three terminals, that is, source, drain and gate and the voltage of source electrode is normally zero. The voltage between drain and source is called gate voltage (V_g) and the voltage between drain and source is named as source-drain voltage (V_{ds}).

The operating regimes of an OFET device can be divided into two regimes. The initial condition for OFET is source-drain voltage setting with zero, source electrode is grounded and gate voltage is connected with a constant value, which can be either positive or negative. In the case of positive gate voltage applying, negative charges (electrons) will accumulate at the semiconductor and dielectric interface. While with negative voltage, positive charges (holes) will accumulate.

First, it is the linear regime, which starts with an increasing source-drain voltage from zero, and ends with source-drain voltage reaches "pinched off" point. The "pinched off" point is a special value for the source-drain voltage starting to form depletion region and at this specific voltage, the next saturation regime starts, shown in Figure 2.2. To be more clearly, the point can be illustrated with an equation,

$$Vd = Vg - Vt \qquad \text{(Equation 2.1)}$$

where Vt is the threshold voltage. From the equation, it is easy to see when source drain voltage equals to the difference between the gate voltage applying and the threshold voltage, then channel is "pinched off". The reason why the concept of threshold voltage comes up is to satisfy the prerequisite of current flowing in channel, which is to fill in deep traps in channel with charges. Then the additional charges are able to move and come to being current. Therefore, linear regime forms on the condition that small source-drain voltage applies ($Vd \ll Vg-Vt$) and the current flowing is driven by Vd from drain to source electrode and the value is in directly proportional to Vd.

The second and final regime is saturation regime, which forms by continuing increasing the source-drain voltage. Reaching Vd=Vg-Vt, channel is "pinched off". Increasing further, depletion region forms from "pinched off" point to the drain electrode area and the difference between local potential V(x) and gate voltage is below threshold voltage. At that time, a space-charge limited saturation current can flow cross the depletion region by high electrical field[1]. From now increasing source-drain voltage only expand the depletion region, instead of the current going up. Since the point is decided by Vg and Vt, the potential difference between the point and the source will not change, leading to saturation regime.

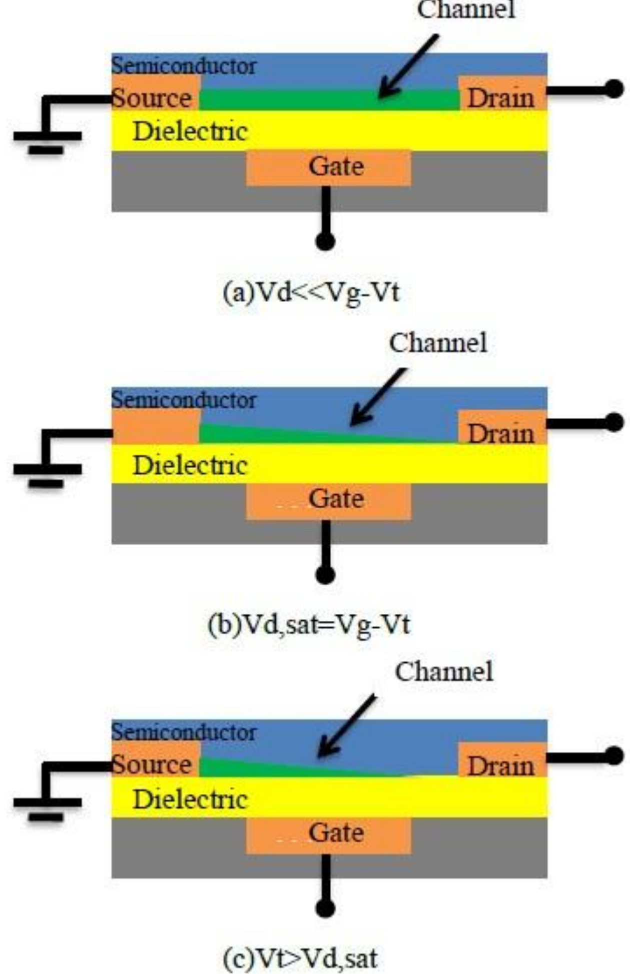


Figure 2.2. Illustration working principle of the an BC/BG OFET**.** (a) Linear regime. (c) The pinch-off point at the beginning of the saturation regime. (d) Saturation regime further. Color indication: Gray: silicon substrate. Yellow: Dielectric layer. Blue: organic semiconducting layer. Orange: Metal electrodes. Green: Charge carriers transport in the channel

2.2 Current-voltage relationship

The field effect transistor (OFET) using its dielectric layer have the same working principle as a capacitor. It is characterized by capacitance C, which equal to the ratio of charge ±Q on each conductor to the voltage V between them. Hence, the mobile charges per unit area (Qi) can be illustrated by equation, which is proportion to the capacitance per unit area (C_i) and the gate voltage (Vg)

$$Q_i = C_i V_g \qquad \text{(Equation 2.2)}$$

However, as we mentioned in earlier section, a gated voltage needs to fill the traps first, which means it has to higher than threshold voltage. So the difference voltage between gate voltage and threshold voltage is the voltage really works in this electrical field. Besides, the channel potential (V(x)) also needs to be taken into account. Then the equation turns into

$$Q_i = C_i(V_g - V_t - V(x))$$ (Equation 2.3)

Source-drain current is defined as multiplying current density (J) by cross-section area (A)

$$I_d = J \cdot A = J \cdot W \cdot H$$ (Equation 2.4)

In Ohm's law, current density (J) can be presented by equation:

$$J = \sigma \cdot E$$ (Equation 2.5)

where E is electric field, σ is conductivity of the material. Conductivity (σ) satisfies with

$$\sigma = \mu \cdot Q_v = \mu \frac{Q_i}{H}$$ (Equation 2.6)

where μ is the charge mobility, Q_V is the mobile charges per unit volume.
Combining equation 2.4, 2.5 and 2.6, source-drain current can be obtained by the following equation,

$$I_d = W \cdot \mu \cdot Q_i \cdot E$$ (Equation 2.7)

According to equation and further substituting E=dV/dx, I_d can be written into

$$I_d \cdot dx = W \cdot \mu \cdot C_i \cdot (V_g - V_t - V(x)) \cdot dV$$ (Equation 2.8)

Then with integration, x from x=0 to x=L, corresponding to V from V(x) = 0 to V(x) =V_{ds},

$$\int_0^x I_d \cdot dx = \int_0^{V_{ds}} W \cdot \mu \cdot C_i \cdot (V_g - V_t - V(x)) \cdot dV$$ (Equation 2.9)

Hence, source-drain current:

$$I_d = \frac{W}{L} \cdot \mu \cdot C_i \cdot [(V_g - V_t)V_d - \frac{V_{ds}^2}{2}]$$ (Equation 2.10)

When Vd<<Vg-Vt, $Vds^2/2$ can be ignored and the equation is simplified to

$$I_d = \frac{W}{L} \cdot \mu_{lin} \cdot C_i \cdot (V_g - V_t) \cdot V_d$$ (Equation 2.11)

The equation is adequate for linear regime. In linear regime, Id is in proportional to Vg and the mobility can be extracted from the slop of Ids vs. Vg at constant Vds, shown in equation

$$\mu_{lin} = \frac{\partial I_d}{\partial V_g} \cdot \frac{L}{W \cdot C_i \cdot V_{ds}}$$ (Equation 2.12)

When Vd ≥ Vg-Vt, Vd needs to substitute by Vg- Vt due to the channel is pinched off and the current cannot increase anymore, yielding

$$I_{d,sat} = \frac{W}{2L} \cdot \mu_{lin} \cdot C_i \cdot (V_g - V_t)^2$$ (Equation 2.13)

and the mobility in saturation regime is obtained

$$\mu_{sat}(V_g) = \frac{\partial I_{d.sat}}{\partial V_g} \cdot \frac{L}{W \cdot C_i \cdot (V_g - V_t)}$$ (Equation 2.14)

Charge carrier mobility is one of the most important performance parameters of OFET devices, which indicates how fast holes or electrons move within a material in an electric field. It is measured in cm^2/Vs. To maximize the transport speed of a transistor, the value of carrier mobility should be as large as possible and channel length should be as short as possible. Mobility strongly depends on the dielectric interface and the organic semiconductor morphology at this interface. Furthermore, it varies with temperature and contact resistance.

Figure 2.3(a) show the typical output characteristics which indicates drain current versus source drain voltage in different gate voltages condition. Figure 2.3(b) exhibits a typical transfer characteristic which refers to drain current versus gate voltage at constant source drain voltage. From these characteristics, the feature of charge transport in the interface between semiconductor and dielectrics can be demonstrated.

The output curves are plotted with increasing negative source drain voltage and the current is corresponding negative. It exhibits an obvious linear regime and saturation regime when looking at single curve at constant V_g. the current starts with linear proportion to V_{ds} and then move to horizon at high V_{ds}, that is, saturation regime. Furthermore, the drain current increase with gate voltage, which means a large density of charge carriers accumulated with high gate voltage.

The transfer curve is plotted with absolute value of drain current and the root of drain current as longitudinal coordinate separately. The transfer curve with the square root of the drain current can yield threshold voltage. The reason can be illustrated by equation 2.15. With square root of both side of the equation,

$$\sqrt{I_{d,sat}} = \sqrt{\frac{W}{2L} \cdot \mu_{lin} \cdot C_i} \cdot (V_g - V_t)$$ (Equation 2.15)

The equation shows a linear relation between $\sqrt{I_{d,sat}}$ and the gate voltage. And $Id^{1/2}$ vs. Vg plot gives a straight line with the slope proportional to mobility. At low gate bias a deviation from the straight line appears which is attributed to the decrease of the mobility caused by trapping of carriers at defect sites. At increasing gate bias, a higher concentration charges at the interface between semiconductor and dielectrics to fill trap states and additional charges induce higher mobility along the channel. The threshold voltage is obtained by extra linearity The threshold voltage is decided by the semiconductor and dielectrics due to the impurities and charge trapping sites tending to increase the value. Hence, it is affected by the factor of built-in dipoles, purity, interface state and trapping issues etc. [2]

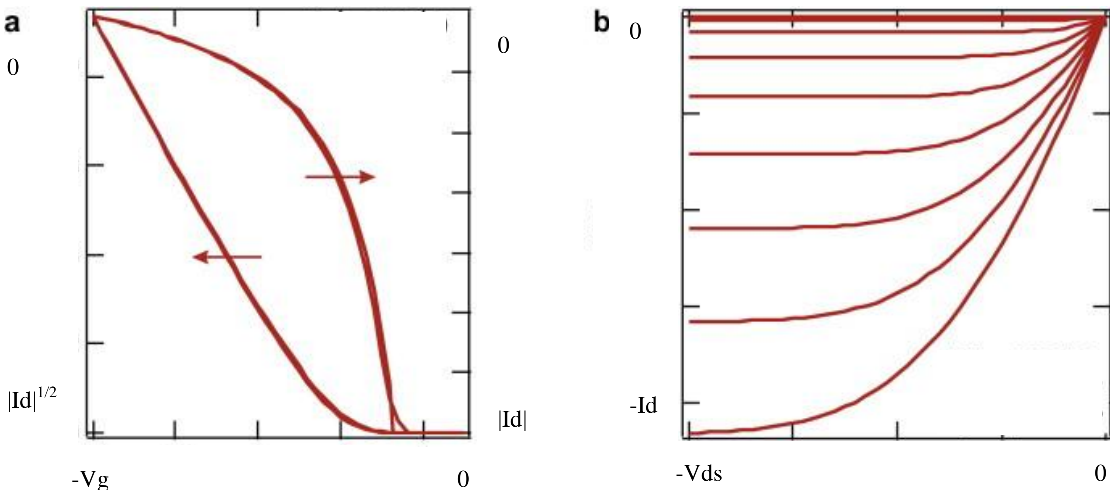


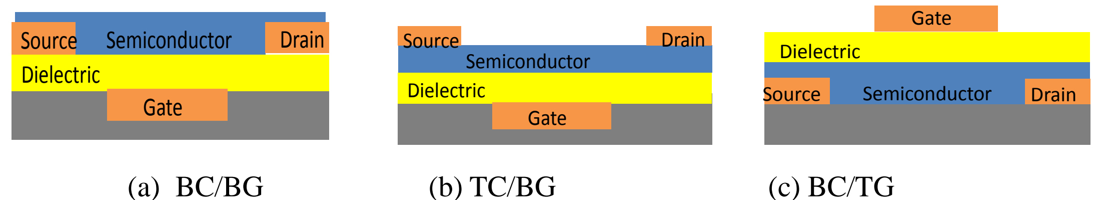
Figure 2.3. Typical transfer (a) and output characteristics (b) of an OFET.

To get the desire curve and current, there are some requirements need to be stratified. The channel length should at least 10 times larger than the dielectric thickness, that is, L>10d, which can ensure gate voltage determining and controlling the charge distribution in the channel. [3] In this project, dielectric thickness is equal to 400nm and the minimum channel length designed is 5μm. hence, all the channel is larger more than12.5 times compared to dielectric thickness.

From the equation above, it is obvious that the current can be enhanced by increasing dielectric constant or decreasing the thickness (d). It means that long channel length can derive high mobility. Hence, the device with 25μm channel length is expected to have better performance.

2.3 Device configuration

There are three common used OFET configurations, which are Bottom Contact/Bottom Gate (BC/BG), Top Contact/Bottom Gate (TC/BG), and Bottom Contact/Top Gate (BC/TG) configurations.



(a) BC/BG (b) TC/BG (c) BC/TG

Figure 2.4. Three OFETs configurations: a) Bottom Contact/Bottom Gate (BC/BG); b) Top Contact/Bottom Gate (TC/BG); c) Bottom Contact/Top Gate (BC/TG)

For the Bottom Contact/Bottom Gate (BC/BG) configuration, dielectric layer is on the top of gate. Drain and source electrode are deposited on the dielectric layer. Semiconducting layer is cover the drain, source electrode and dielectric layer. It has gate electrode on the bottom and the other two electrodes conducting semiconducting layer from bottom, thus it is called BC/BG configuration. Correspondingly, TC/BG configuration has gate electrode on the bottom and the drain/source electrodes conducting semiconducting layer from top, BC/TG configuration has

gate electrode on the top and drain/source conducting semiconducting layer on the bottom.

These three configurations result in different advantages and disadvantages, including working performance, fabrication method and so on, and BC/BG and TC/BG configurations are more commonly used, which is also the two configuration used in this project. As to working performance, the contact area between organic layer and drain/source electrodes is different. In BC/BG configuration, charges are injected from the sidewall of electrode, causing high injection resistance whereas charges are injected from both the edge and surface of the electrode in TC/BG and BC/TG configuration. It indicates that the performance of TC/BG and BC/TG configurations is superior to BC/BG. However, in BC/BG configuration, charges can be directly injected into the channel, which at the semiconductor-dielectric interface. While in TC/BG and BC/TG configuration, semiconducting layer is between source/drain electrodes and the channel, which means charges have to travel through organic material then reach the channel.

As to fabrication method, in TC/BG configuration, source and drain electrode need to deposit onto semiconductor layer, thus another technique is introduced, that is, deposition electrode with nanostencil, which can avoid the organic layer damage from photolithography process.

2.4 Unipolar and Ambipolar OFETs

2.4.1 Energy level

In this project, organic semiconductor material has been used. Compared with Inorganic semiconducting material, normally referring to IV Silicon and Germanium and III-V compounds like Gallium-Arsenide and Gallium-Nitride, organic semiconductors attracts more attentions. One of the main features of this class of material is the chemical synthesis of the molecular building blocks. It makes the material can be tailored to satisfy with special purposes of applications, such as modification of the color of the luminescence output. Together with the properties of low cost, uncomplicated processing methods, including solution deposition or by vapor deposition, flexible substrates possible, organic semiconductor becomes a promising candidate for organic light-emitting field-effect transistors. [4]

As organic semiconducting material, the energy level correspond to valence band and the conduction band, known as highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), [5] it is easy to known that among the occupied molecule orbitals HOMO is the molecule orbital with highest energy and among the unoccupied molecule orbitals LUMO the molecule orbital with lowest energy.

It is easier to understand the HOMO and LOMO theory starting from band theory in inorganic semiconductor. The unique electric conductive behavior of semiconductor, differing from metal and insulator, can be illustrated by its energy gaps, which refers to the energy difference between the top of the valence band and the bottom of the conduction band. The reason why

metal have good conductivity is the two bands are overlapped that make electrons can move freely with little energy cost, while band gap of insulator is quite large to let electron motion. As to the semiconductor, conductivity is between metal and insulator, which determined by the free electron and holes, known as charge carriers. Adding excess electrons or excess holes into a inorganic semiconductor can increase its conductivity and create corresponding n type or p type semiconductor.

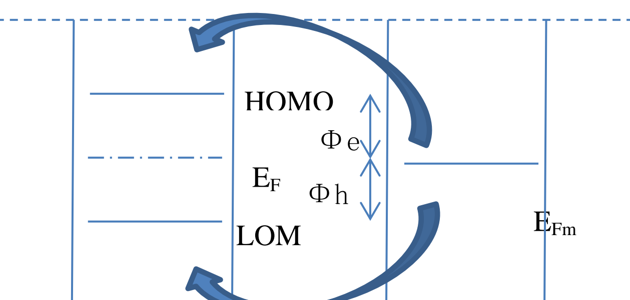


Figure 2.5. Energy level diagram of an OFET.

Considering the energy level relating to organic semiconductor, Figure 2.5 shows energy level diagrams of a metal and organic semiconductor separately. When voltage bias applies between organic semiconductor and metal electrodes, Charge carriers start to move between these two materials and in the end the two Femi level will keep in same level. If the work function of metal electrode is between HOMO and LOMO, holes can be inject to HOMO which will introduce a hole injection barrier Φh level while electrons inject to LOMO level which will introduce electron injection barrier Φe. Φh is the energy difference from the metal work function to the HOMO level of organic semiconductor, while Φe is the energy difference between metal work function to the LUMO level of organic semiconductor.

According to charge carrier's transport in the channel, organic field effect transistor can be classified as p-channel and n-channel. If in the organic semiconductor holes mainly transport to HOMO level, it is defined as p-channel. Likewise, if electrons mainly transport to LOMO level, it is defined as n-channel. Both two cases called unipolar transport. There is also a third case when both electrons and holes transport from metal to organic material, which is called ambipolar transport [1].

During the charge transport, an ohmic contact is formed when the work function of metal and the LUMO or HOMO level match well which can improve charge transport. While when the work function of metal and the LUMO or HOMO level couldn't match well, a Schottky barrier is formed to block charge carries transport.[6][7]

2.4.2 Unipolar OFETs

In theory, both electron and hole conduction should be supported equally.[8] However, most of OFETs exhibits unipolar charge transport, typically p-channel, conducting holes better than electrons.[9] When organic semiconductor connects with high work function metal, holes tend to inject more easily, known as p-channel transistor. Among many organic semiconductor

HOMO level ranges from 4.8ev to 5.3ev, which leading to good match with high work function metal, like gold (5.1ev). By contrast, when organic semiconductor connects with low work function metal, electrons are prone to inject to the channel, known as n-channel. However, n-channel OFET has its limits compared to p-channel, resulting from the drawbacks of low work function metal. For many organic semiconductors, LOMO level is around 2-3ev, and corresponding metal aligned has to be metal like, calcium and magnesium. They are unstable and reactive even with bare air. For example, calcium (Ca) with 2,87ev low work function can rapidly form Calcium oxide (CaO) when exposed to air and produce hydrogen when meet with water, which makes it hard to use as metal electrode in OFET.

Therefore, in this project, aluminum is considered as a promising candidate material with the work function of 4.28 eV. It is a compromised choice between low work function and stability. Through a thin surface layer of aluminum oxide will form if the metal is exposed to ambient air. It still can be used in TC/BG configuration to investigate its n-channel behavior.

There are some possible solutions for n-channel transistors. One is lower the LOMO level of organic semiconductors, which can be achieved by adding molecule with high electron affinity such as fullerene and their derivatives, the other is protecting low function metal by adding protecting layer or conducting in vacuum condition. There an another challenge for n-channel is hydroxyl groups in gate dielectric as discussed in section, for elections are more easier be trapped as SiO^- ions.

The organic semiconductor can either be investigated as non-crystalline thin films and crystalline nanofibers. And in this project, thin film PPTTPP works as the organic semiconductor layer.

Phenyl thiophene co-oligomers, represented by PPPTTPP oligomer, from literal which means it contains both thiophene and phenylene group. And PPTTPP is that kind of hybridised oligomer, consisting of two thiophenes in the center and each side two phenylene in flank, shown in Figure 2.6. Hybridising and blending of materials on a molecular level is an effective method to improve desired properties, and Thiophene/phenylene co-oligomers have been shown promising application potential in future optoelectronic devices, like organic field effect transistors (OFET).[10][11]

Figure 2.6. Chemical structure of PPTTPP molecule

The HOMO and LUMO level of PPTTPP have been reported by Gao, H et al. according to their photoemission spectroscopy result, the HOMO and LOMO are 5.3eV and 2.8eV respectively.[36] The metal used in this project is gold (Au) with high work function around 5.1eV and aluminum (Al) with lower work function 4.28 eV. Therefore, the work function of

gold is close to HOMO level of PPTTPP, which means that holes working as the majority charge carriers transport to HOMO level. Base on that, the device can be predicted as the result of p-channel OFET. Although the work function of aluminum is also close to HOMO level, this metal gives greater chance for electron transport. Hence, OFET device with Al electrode is expected holes as well as electrons transport in the channel..

2.4.3 Ambipolar OFETs

Ambipolar OFETs indicates that electrons as well as holes can be accumulated in the channel by applying voltage. Assuming a positive gate voltage is applied and starting with equal of source drain voltage. If the gate voltage is larger than the threshold voltage of electrons, the gate is more positive than the source, which is grounded leading to electron injected from source, which is drifted towards drain. Only one polarity of charge carries in this case named unipolar regime. On the other hand, if gate voltage is smaller than the threshold voltage of electrons, the drain electrode will inject hole to the channel with no electrons injected by source. Taking the absolute value of the voltage difference between drain and gate as well as the threshold voltage of holes, if the former is larger than the latter, namely $|V_g - V_{ds}| > |V_{t,h}|$ and at the same time the gate voltage is larger than the threshold voltage of electrons, both electrons and holes are injected to the channel and further an opportunity to emit light.

Figure 2.8 shows the transfer and output characteristics of an ambipolar OFET.[1] the transfer curves is obtained by sweep a positive gate voltage with different positive source-drain voltage applied, show a V-shape, one arm suggesting the electron transport and the other suggesting hole transport. Moreover, depending on different source-drain voltage, the curve has been raised. As to output characteristic, the curve sweeping both to the negative and positive indicating different charge carriers working at higher voltage compared to lower voltage

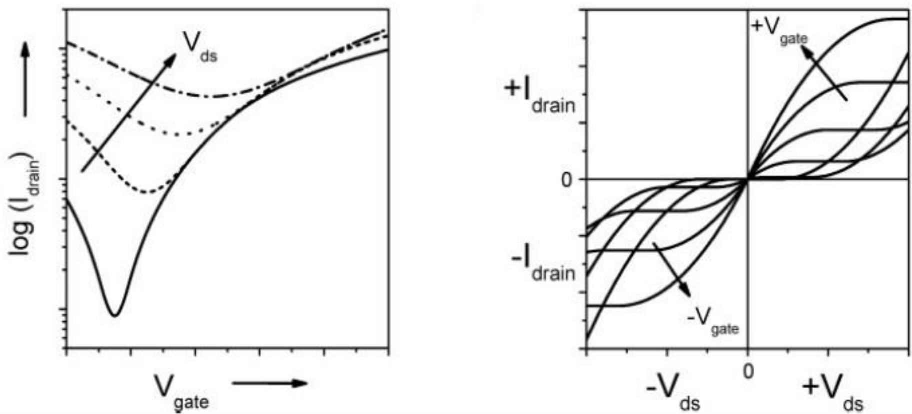


Figure 2.8. (a) Transfer characteristics for an ambipolar transistor; (b) output characteristics for the same transistor for positive (first quadrant) and for negative (third quadrant). Taking from ref.[1]

The challenge of fabricating ambipolar OFETs is in several respects. One thing is its aligning

the work function of metal electrode to the semiconductor. Since the band gap of normal organic semiconductors is around 2-3ev, it limits the possible metal material into a few. Another thing is trapping issues, including one or two carrier types. It can be solved by suitable dielectrics and an inert processing environment.

2.5 Organic Light-Emitting Transistor (OLET)

Light-generation devices have developed in a rapid way in past decades, organic light-emitting diodes (OLEDs) [4] and organic light-emitting field-effect transistors (OLETs) are the evident cases.

OLED contains a cathode and anode layer sandwiched by a single or multiple active organic layers. The working principle can be simplified as: when a voltage is applied, the electrons are generated by cathode and holes are injected by anode. The combination of them cause light-emitting. The limitation of the OLED is that as a vertical structure the two electrodes need to be transparent to emit light outside, which requires some specific material to act as electrode. Besides, it is also difficult to characterize the light generation.

OLETs utilize active organic layer emitting light. By contrast, the planar structure OLETs show its superiority compared to OLEDs. Moreover, the life time and efficiency of OLETs can be enhanced by different charge carries situations with respect to standard OLED architectures.

Hepp et al. reported the first organic light-emitting field effect transistor in 2003 based on BC/BG configuration with tetracene polycrystalline film as organic semiconductor.[12] The electrical device characteristics shows typical of a unipolar p-type curves, and emitting light is observed in the area close to drain, which give the evidence of electrons and holes are injected into the tetracene layer. However, only one type charge carrier is involved into transport and only the area t near the minority carrier injection electrode can be generated with light, which lead to the low efficiency light emission in unipolar transistors.

In contrast to unipolar OLETs, ambipolar OLETs improve the efficiency of recombination of charge carriers by injecting both electrons and holes. In this section, the two different operation methods are discussed, one is DC gate voltage operation, and the other is AC gate voltage operation, presented by Yamao et al. in 2008. [13]

2.5.1 Direct-Current (DC) Gated Ambipolar OLETs

Similarity with the discussion of section 2.4.2, the operating regime can be classified to three types, including unipolar regime for electrons, unipolar regime for holes and ambipolar regime. Figure 2.9 shows the working principle of ambipolar light emitting transistor, starting with applying a lower negative gate voltage Vg, a higher negative source-drain voltage compared to Vg and grounded source voltage. Hence, electrons flow from drain electrode and occupy the whole channel at the beginning, at that time the gate voltage is below threshold voltage and no holes injected. In Figure 2.9 (b), gate voltage reaches the threshold voltage and holes begin to

be injected from source electrode. Here electrons channel and holes channel meet each other and intrigue light emitting. As gate voltage decreasing more, the absolute gate voltage increasing more and emission line moves from source to drain in the meantime. At a point, emission line will reaches drain electrode and holes occupy the channel, shown in Figure 2.9(c)

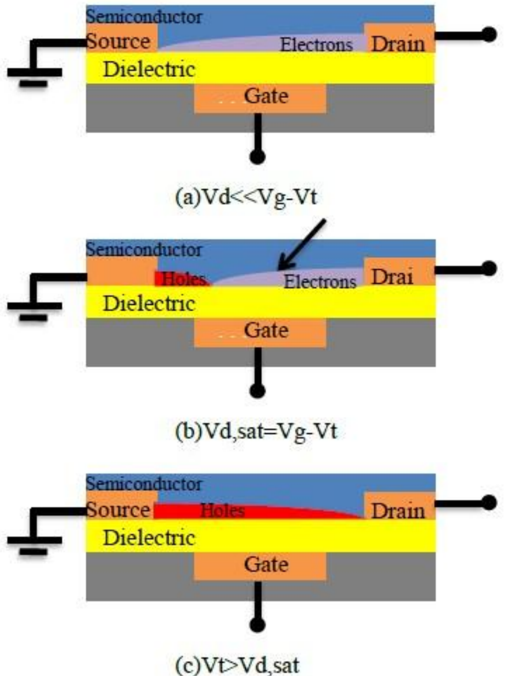


Figure 2.9. Schematic diagram of operating working principle in DC voltage gated ambipolar OLET

2.5.2 Alternating-Current (AC) Gated Ambipolar OLETs

Operating circuit of AC gated ambipolar OLET is shown in Figure 2.10. Source is connected with a negative constant DC voltage Vs, drain electrode is connected with positive constant DC voltage Vd. And gate electrode is applied with AC voltage with frequency f and amplitude V_G, following the relation $Vg=V_G\sin(2\pi ft)$ with $V_G>Vd$ and $V_G>|Vs|$.

Assuming the gate voltage applying starts from $Vg= -V_G$, the bottom point, the situation at this moment is drain more positive than gate, thus causing holes dominate the channel. Then when gate voltage increase to –Vs, no potential difference between source and gate, which is the pinch off point. As the gate voltage increase to a positive voltage, the source electrode starts to inject electrons due to the source is more negative than the gate. Hence, holes and electrons can be recombined here and thereby emitting light.

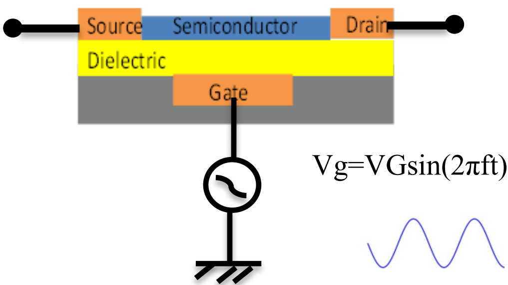


Figure 2.10 Schematic diagram of operating circuit in AC voltage gated ambipolar OLET

CHAPTER 3 DIELECTRIC MATERIALS

Dielectric materials play an important role in organic light-emitting transistors (OLETs). The working principle of OLETs can be simplified as holes and electrons meeting to recombine and emit light. And the recombination is restricted by some issues from dielectric layer, including dielectric constant and trapping-sites. Dielectrics affect the morphology of organic semiconductors. Increased roughness of interface can cause valleys in the channel region, which may work as carrier traps. The most commonly used gate dielectric silicon dioxide (SiO2) is expected to trap electrons and thereby prevent their transport through the transistor. Therefore, the integration of a different gate dielectric is required. And the polymer dielectrics is mainly been investigated in this project, which is expected to improve the device performance via reduced charge trapping and thereby result in higher energy efficiency.

3.1 Working principle

Dielectrics is the material undergo a slightly shift in charge positions when electric field applied, resulting to dielectric polarization. Due to this process the positive and negative charges are moved to two opposite electrical field direction forming internal electric field. Dielectrics normally work as an insulating layer of either capacitor or transistors. As a capacitor, dielectric material is sandwiched by two electrodes. There is a large band gap in dielectrics and when electron is excited through the band gap the dielectric material is broken down and loses its insulating properties, which requires sufficient energy and differ from materials. In real capacitor, dielectric is not completely insulating and allows flowing through small amount of current, which is called leakage current. In this project, we focused on the application of field effect transistor with adding semiconductor layer and another terminal.

Dielectric materials are mainly characterized by the absence of charge transport [1]. Assuming two electrode are separated with thickness d in vacuum and a voltage applied between them to create electric field, the charge per area is

$$Q = \varepsilon_0 E = \frac{\varepsilon_0 V}{d} \qquad \text{(Equation 2.1)}$$

And capacitance can be written as

$$C = \frac{Q}{V} = \frac{\varepsilon_0}{d} \qquad \text{(Equation 2.2)}$$

Inserting a dielectric material between the electrodes, the capacitance is increased by factor k, which is the dielectric constant, and the capacitance per unit area is described by equation:

$$C_i = \frac{k\varepsilon_0}{d} \qquad \text{(Equation 2.3)}$$

For OFET devices, a high dielectric constant and low thickness is desired to achieve a high

capacitance with gate dielectrics, thereby producing low voltage operating OFETs.

3.2 Gate dielectric materials

3.2.1 Silicon dioxide

Silicon dioxide has been used as dielectric layer for decades, which dielectric constant is 3.9. One reason attributed to its popularity is the available silicon technology. High quality and smooth silicon dioxide can be directly obtained by Si wafer by means of thermal oxidation silicon which can provide with reproducible results for many transistors. However, silicon dioxide have reaches its material limits, which require some improvements or exploring new materials to replace it.

First, the dielectric constant of silicon dioxide is relatively low, around 3.9. According the equation, the capacitance is determined by the factor dielectric constant k and thickness d and high capacitance is required to drive current and enhance device performance. In order to increase capacitance of dielectric material with lower dielectric constant, the thickness of silicon has to scale down. However, leakage current increases exponentially on the condition that the thickness decreases and it increase drastically as the thickness comes to 2 nm. The OFET devices with large leakage current not only consume high power but also reduce its reliability. For the capacitor with silicon dioxide, when applying the voltage of 1V the leakage current based on 3nm SiO2 is around 10^{-5} A/cm2, while the leakage current based on 1.5nm SiO2 is around 10 A/cm^2, 10^6 times larger.[1]

Therefore, high-k materials should be employed to minimize leakage current. The good performance of the OFET devices should be obtained by considering both dielectric constant and thickness of dielectric material.

Second, it has been demonstrated that at the interface between silicon dioxide and semiconductor large density of electrons is trapped by hydroxyl groups in the form of silanols.[3]

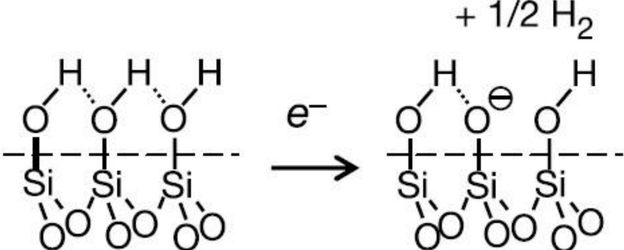


Figure 3.1. Schematic diagram of charge trapping mechanism at the interface between silicon dioxide and semiconductor. Taking from ref.[3]

Figure 3.1 shows the mechanism of -OH groups trapping electron. In n-channel field effect

transistors, electrons are trapped to generate SiO- ions, which quench the n-channel OFET activity

One of the solutions reported by Friend et al. is using self-assembled monolayer (SAM) [3]. It can be clear seen from the figure 3.2, that silicon dioxide substrate with SAM- modified reduce the density of electron-trapping groups, thereby developing the mobility. Meantime, the leakage current is decreased to the order of 10^{-8}A/cm^2, compared to the leakage current with SiO2 layer on the order of 10^{-3} to 10^{-1} A/cm^2. With self-assembled monolayers (SAMs), like alkylsilane, the chlorine atoms combine with hydrogen atoms of silicon dioxide to form hydrochloric acid, thereby creating monolayer to remove electron trapping site, illustrated by Figure 3.2.

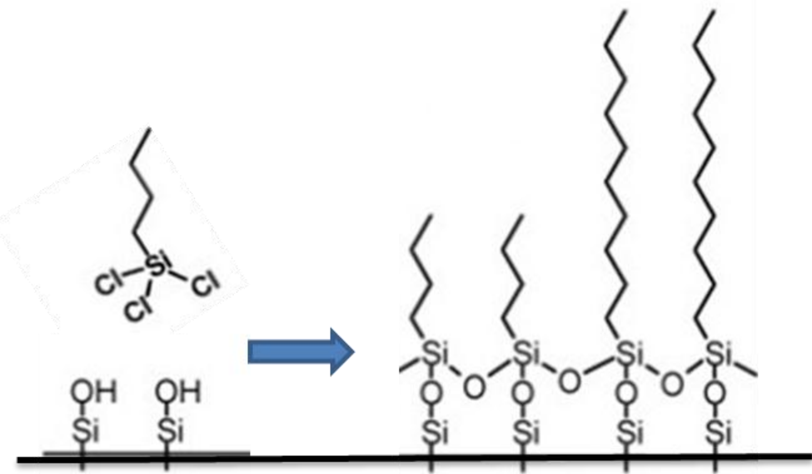


Figure 3.2. Schematic diagram of the formation of alkylsilane SAMs. Talomg from ref.[5]

In work of Chua and coworkers, several alkyl SAMs and polyethylene (PE) were used as buffer layer on SiO_2 to investigate the electron-trapping situation.[3] In detail, the SAMs passivation are HMDS, DTS and OTS which is the abbreviation of hexamethyldisilazane (C_1), decyltrichlorosilane (C_{10}) and octadecyltrichlorosilane (C_{18}). It indicates that these three alkyl-SAMs (HMDS, DTS and OTS) with alkyl chains of one, ten and eighteen carbon atoms respectively. [14] The measurement was conducted starting with an initial sweeping to fill some traps, then obtaining the transfer characteristics of the second gate voltage sweeping. From the result shown in the figure 3.3, n-channel FET activity is not found on pristine SiO2. While as to treated-SiO2, n-channel activity can be observed with gate threshold shifting, which longer chain SAMs can restrain the rate of shifting. It suggests that SAMs cannot eliminate all the SiOH groups on the surface of silicon dioxide, which means remaining –OH groups still exist and it also proves the interfacial trap mechanism mentioned earlier. Moreover, it should be noticed that the device with PE as buffer dielectrics exhibits stable n-channel conduction, which lead to polymer dielectrics can be a promising choice and it will be discussed in later sections.

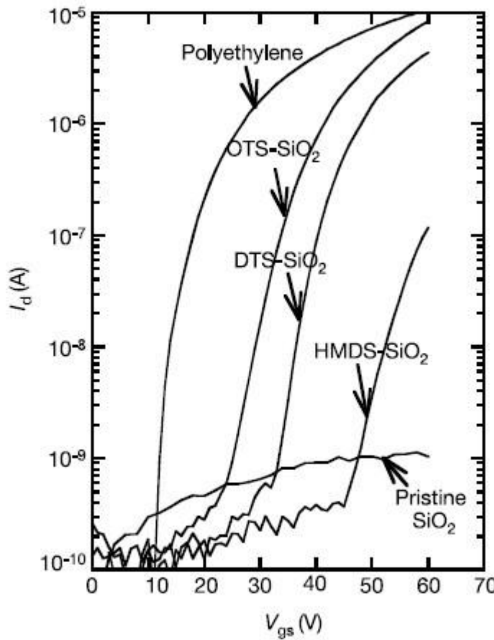


Figure 3.3. Transfer characteristics based on F8BT n-channel FETs with various siloxane self-assembled monolayers (SAMs) on SiO2 as dielectric, or with polyethylene as buffer dielectric. Taking from ref. [3]

It also been reported that using cleaning method of oxygen plasma treatment compared with solvent cleaning diminish contamination at semiconductor-dielectric interface, thereby alleviating trapping effect. [15]

3.2.2 Polymer materials

However, investigating other dielectric materials to avoiding the undesirable properties of silicon dioxide will be the most interesting and promising solution. Considering the option of other dielectrics, there are three strategies:

One is replacing with high-k inorganic materials, which is widely used in inorganic electronics. Despite the high capacitance and low voltage operation can be achieved, even realizing low operate voltage to 5V in BST, Ta_2O_5, Al_2O_3, etc. materials. [16][17][18] This kind of metal oxide has some unavoidable shortcomings. To begin with, the fabrication process contains high temperature annealing processes and high cost deposition process, which leading to inapplicable in plastic substrate and industrialization. Furthermore, for flexible substrates, lack of mechanical properties in general is another unfavorable property. The last but not the least, hydroxyl (–OH) groups generally exists in these high-k oxides, causing the undesirable semiconductor-dielectric interface thereby exhibiting inferior properties of mobility, stability and leakage current.

The second is replacing with polymer dielectrics. It provides with relative low dielectric constant, good mechanical properties, and simple process to deposit. Nevertheless, some constraints still limit it from wide applications, including high thickness to minimize the

leakage current, usually acceptable current can be achieving when the thickness of gate dielectric is larger than 300nm[19] and their generally high operating voltages, typically larger than 20 V, because of the capacitance of high thickness gate dielectric is usually lower than 15nF/cm^2 and large density of defect state in organic semiconductor layer and semiconductor-dielectric interface.[20] Besides, polymer dielectrics can be used in both top and bottom gate transistor. For top gate transistor, Polymer gate dielectrics do not interfere with the morphology or damage the semiconductor via spinning on the top.

For organic transistors, the desired property of dielectric layer should be low thickness, pinhole-free, and with a high dielectric constant for low voltage operation.

Cross-linked polymers are demonstrated to be a solution to improve the properties of polymer dielectrics. The desired cross-linked polymer possess the properties of smooth surface (root mean square roughness less than 1 nm), high electrical field strength, large dielectric constant preferable, high level of purity, high hydrophobicity with enough adhesion to neighboring materials, which can exclude chemical structure like Teflon.[21] Yoon et al. have utilized cross-linked PVP to create ultrathin thickness.[19]It is reported cross-linked polymer blends (CPBs) forms by using PVP and PS two polymers and several cross-linking reagents, shown in Figure 3.4. The cross-linking of the polymer dielectric enables depositing subsequent layers via spin-coated or printed. These CPBs shows the capacitance of 200-300 nF cm^{-2} with 10-20 nm thin layer, exhibiting large k/d ratio and low leakage current (leakage current is around 10^{-8} A/cm^{-2}. Furthermore, these dielectrics are compatible with n$^+$-Si, ITO, and Al gates and various p-type and n-type semiconductors. They also possess another pursuing property of pinhole-free.

When polymer dielectric is modified by self-assembled monolayers and multilayers, OFET devices also can achieve low thickness, high capacitances and improve its performance

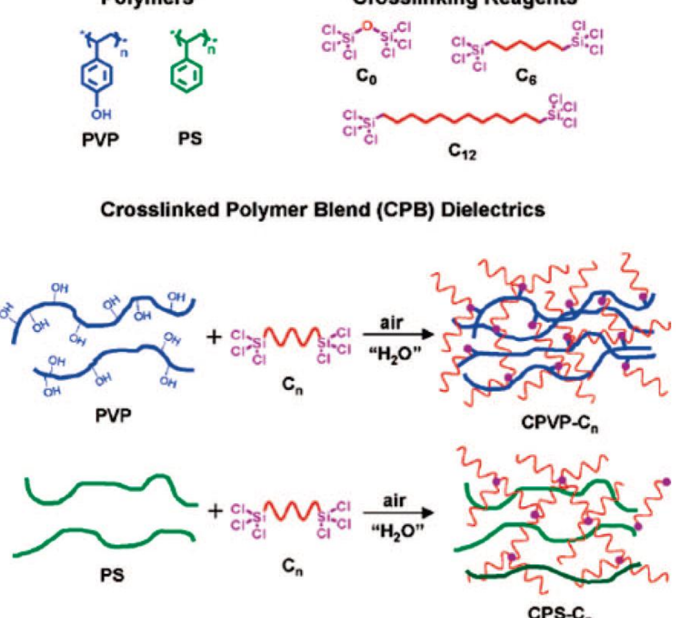


Figure 3.4. Schematic diagram of the synthesis of cross-linked polymer bends (CPBs). Taken from ref.[19]

Curing environment is another factor can be improved, which proved by Hwang and his coworkers in the case of PVP. [22] In their work, measurements conducted on the condition of vacuum or Ar gas flow, based on the different surface properties of dielectric material can be generated under various curing conditions. Under vacuum environment, PVP process lower surface energy than the case under Ar gas around. Furthermore, the corresponding mobility under vacuum is higher than the case under Ar. It is reported that the performance of pentacene based thin film transistors have been enhanced

The third is replacing with hybrid inorganic-organic dielectric, including polymeric-nanoparticle composites, inorganic-organic bilayers, and hybrid solid polymer electrolytes.

In this project, we focus on investigating promising polymer dielectrics. Polymer organic material working as gate dielectric layer in OFET device was first successful utilized by Peng et al. in 1990.[23] weighing the advantages and disadvantages of various polymer material, there are some promising candidates. They are polymethyl methacrylate (PMMA), polystyrene (PS), polyimide (PI), poly 4-vinyl phenol (PVP), benzocyclobutene (BCB), polyethylene (PE) etc.

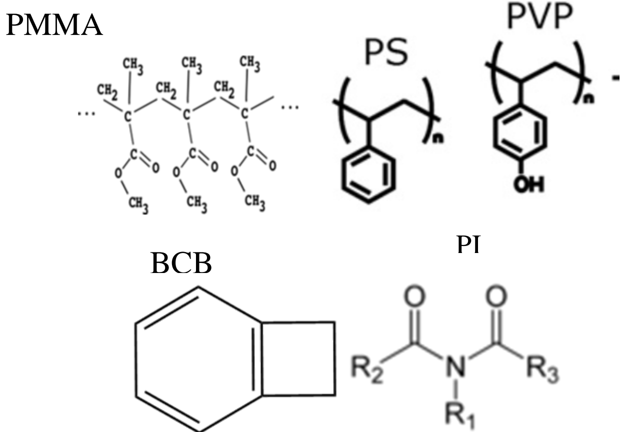


Figure 3.5. Chemical structures of polymer dielectrics. Taking from ref[1]

(1) Poly 4-vinyl phenol (PVP)

It is reported that OH groups in the buffer dielectric will hinder electron transport [1], which means that PVP should not support electron transport. poly 4-vinyl phenol (PVP): contain benzene rings attached on the side chain of polymers with hydroxyl groups. Hence, PVP needs to be cross-linked first [24]. Yang et al have reported pentacene OFETs using cross-linked PVP as gate dielectric gives a high mobility. [25]

However, even if –OH group have been replaced by crosslink agents, cross-linked polymer cannot ensure all –OH groups have been removed. The reason is the absorbed water which may move into the channel area via the boundaries of grain and few remaining –OH group can create trapping site thereby forming new hysteresis and degrading the device performance.[26][27]

Therefore, the functional groups on should be considered as an important parameter to select polymeric gate dielectrics, which will further determine the type of accumulated charge carrier. A hydroxyl-free polymer should be integrated to improve electron conduction in channel of OFETs, such as BCB, PMMA, and PS. Chua and coworkers compared different polymers (BCB, Parylene, PE, PMMA, PVP, and PI). The best polymers for n-type transport are reported to be BCB, Parylene, and PE. [3]

(2) Benzocyclobutene (BCB)

BCB is first reported in 2004 to form tens of nanometers thick thin film dielectric layer by ease solution casting process. [3] The chemical structure of BCB contains a benzene ring attached to abject cyclobutane ring and its chemical formula is C_8H_8. It exhibits some excellent result, including high dielectric breakdown strength (larger than3 MV/cm), low leakage current (less than 10 nA), low fixed charge and trap densities in the bulk and at interfaces. However, due to the high price of BCB, this material cannot be investigated more in this project.

(3) Polystyrene(PS)

Chao Jiang et al. tried with PS [29] which does not contain any hydroxyl groups. The chemical structure is shown in Figure 3.5, containing benzene rings on the chain of polymers. It is obvious that no –OH groups existing, thereby no crosslinks requiring. This kind of structure

offers PS with high stability in air and desirable dielectric property.

(4) Polyimide (PI)

PI has been employed to fabricate high-quality pentacene field-effect transistors by Yusaku Kato. [30] In their work, the mobility was enhanced up to 1 cm^2/V and the films. The surface roughness of PI layer is down to 0.2nm. PI layer can be easily deposited on to the substrate by simply spin-coating and prebake. The curing temperature was reported as 180 ℃. It should be noted that low curing temperature benefit in several respects. Not only simplify the deposition process but also flexible to choose base substrate. This temperature make the material compatible with many plastic films, such as polyethylenenaphthalate (PEN) used in their transistor, which process the feature of low price and good gas-barrier that can protect organic semiconductors from oxidation and absorption of moisture.

(5) Polymethyl methacrylate (PMMA)

PMMA is a polymeric resist with thermal and mechanical stability, high resistivity, suitable dielectric constant, which make PMMA a promising material as a dielectric layer.

The formula of PMMA is $(C_5O_2H_8)_n$, shown in figure 3.5. Standard PMMA products are in 496 K or 950 K molecular weight (MW) in solvent such as chlorobenzene or anisole, which can provide a wide range of thicknesses of PMMA. The recommended coating procedures are spread with the rotation of 500 rpm for 5 followed by ramping to spin speed at a high acceleration rate in 45 seconds. For example, with rotation at 500rpm for 5s and 2000rpm for 45s, 400nm thickness PMMA uniform layer can be achieved. Then 1 minute baking at 200℃ can remove the remaining solvent. Moreover, PMMA is commonly used in high resolution nanolithographic processes, like electron beam lithography (EBL). PMMA has been also used as a protective layer for wafer thinning. Together with the properties of high resistivity, similar dielectric constant with silicon dioxide makes PMMA a promising dielectric material using in OFET devices. [31]

PMMA material working as gate dielectric has been reported with good electrical performance ascribed to the influence of pentacene thin-film microstructure thereby increasing the crystallinity. The pentacene thin-film OFET fabricated by J. Puigdollers et al. shows 0.01 $cm^2 V^{-1}s^{-1}$ mobility and -15 volt threshold voltage. [31]

In short, PS, PI, PMMA can be the possible material to fabricate OFET. However, due to the time-limiting in in this project we only present organic effect transistors with polymethyl methacrylate (PMMA) as the gate dielectric material.

Dielectric material	Chemical structure	Dielectric constant	Properties	Deposition method
Polymethyl methacrylate (PMMA)		3.5	thermal and mechanical stability, high resistivity, suitable dielectric constant	Spin-coating
Polystyrene (PS)	PS	2.6	Widely used in plastic, low melting point, naturally transparent	Spin-coating
Polyethylene (PE)		3.5	high stability, trap-free, large band gap (around 8.8 eV), low conductivity (around $1*10^{-18}$ Ω^{-1} cm^{-1}), low toxicity, chemical inertness, simplicity processing in large-area	vacuum-evaporated deposition
Polyimide (PI)		3.5	thermal stability, good chemical resistance, excellent mechanical properties	Spin-coating
poly 4-vinyl phenol (PVP)	PVP	4.5	A plastic structurally similar to polystyrene. Large k/d ratio, can be cross-linked to remove OH group.	Spin coating
Benzocyclobutene (BCB)		2.65	high dielectric breakdown strength(>3 MV/cm), low leakage current (<10 nA), and low fixed charge. and trap densities in the bulk and at interfaces	Spin coating

Table 2.1. Comparison between possible polymer dielectrics

CHAPTER 4 FABRICATION OF ORGANIC LIGHT-EMITTING TRANSISTORS (OLETs)

This chapter includes the previous experiment to investigate the breakdown voltage of PMMA dielectric layer, design and fabrication of stencil, which is used for deposition fine electrode pair and the fabrication process of the OFET device. OFET devices are fabricated based on different configuration (TC/BG and BC/TG), source and drain electrode (gold and aluminum) and channel length. And the short circuit measurement is also involved acting as a prerequisite of OFET.

4.1 Investigating the break down voltage of dielectric materials

In this project, organic field effect transistors (OFETs) employ polymer dielectric material to isolate between gate electrode and semiconductor layer. As a dielectric material, it is susceptible to the electrical pressure and at a specific amount of voltage, the insulating dielectric begin to flow current. Different form conductors where current tend to be linear with a fixed resistance, in the case of dielectrics the current flow shows a non-linear tendency, which means the current, will flow in a sudden after exceeding the specific voltage. Once the flowing starts, the dielectrics have loose its insulating properties. This voltage is called the break down voltage of the dielectric material.

4.1.1 Work principle

There is a strong relationship between breakdown voltage and the dielectric thickness. [32]The break down voltage can be obtained from the equation

$$V_{bd}= E_{ds}d \qquad \text{(Equation 4.1)}$$

Where E_{ds} is the dielectric strength and d is the distance between the two electrodes. The dielectric strength depends on the intrinsic property of the material, that is, PMMA. So here we investigate how the thickness of PMMA affects the breakdown voltage.

It should be noted that in order to characterize properly of dielectric material, the break down voltage measurement has to be repeatable. Because the break down voltage can be affected by other factors, including involved particles, contamination and environment etc. For example, humidity can decrease the resistance of most dielectrics and alkalis or halides can increase breakdown strength.[32] Moreover, the contamination and involved particles will cause leakage current and charge mobility through insulating area, which the problem meet in the measurement. Therefore the sample need to clean thoroughly and the measures need to conducted in different samples to make sure the value can be trusted.

The device used to measure the breakdown voltage of PMMA in this project works as a capacitor. The two electrodes are separated by PMMA, and PMMA act as the insulator. In practical measurements, there is still a current can be measured below the break down voltage, which is called leakage current. The current can be calculated by the equation

$$I = C\frac{\Delta U}{\Delta t} \qquad \text{(Equation 4.2)}$$

The parameter of $\frac{\Delta U}{\Delta t}$ is the voltage sweep rate, which is used as 0.01V per second and the capacitance per area Ci is given by the equation as follows:

$$C_i = \frac{k\varepsilon_0}{d_{PMMA}} = \frac{3.5 \cdot 8.85 \cdot 10^{-12}}{403 \cdot 10^{-9}} = 7.74 \times 10^{-5}\, F/m^2 = 7.74 \times 10^{-9}\, F/cm^2 \qquad \text{(Equation 4.3)}$$

where the dielectric constant of PMMA k≈3.5, the vacuum permittivity ε_0 = 8.85 x 10^{-12} (F•m−1), the thickness of PMMA is taken 400nm as an example, which is the thickness used to fabricate OFET device and the actual thickness is measured by ellipsometer, d≈403nm. With an electrode area of 0.1 cm^2, the capacitance is obtained

$$C = Ci \cdot A = 7.74 \times 10^{-9} \cdot 0.1 = 7.74 \times 10^{-10}\, F \qquad \text{(Equation 4.4)}$$

Then the leakage current flows can be obtained

$$\mathrm{I} = \mathrm{C}\frac{\Delta \mathrm{U}}{\Delta \mathrm{t}} = 7.74 \times 10^{-10} \cdot 0.01 = 7.74 \times 10^{-12}\, A \qquad \text{(Equation 4.5)}$$

4.1.2 Fabrication Process

The device is fabricated based on the p-doped one side polished silicon wafer with the diameter of 100 µm and thickness of 525 µm. By cutting into 25*25 µm chips, the substrates are ready for fabricating. The configuration of the device contains two electrodes sandwiched by PMMA dielectric layer working as a capacitor, by applying different thickness of PMMA and thereby investigates the break down voltage of them.

The thinner thickness substrates fail to work in the first place due to the short circuit effect. Then the further fabricating process is improved in several respects, including deposition with thickness PMMA and alternative cleaning method to avoid particle left.

It turns out to be the particle issue leading to the short circuit. It involved in following respects: first, cutting procedure requires both photoresist applying and HMDS procedure. The function of photoresist on the wafer is to let the particle caused by cutting left on the photoresist instead of the wafer, while the HMDS procedure is to remain the photoresist on the wafer, otherwise the photoresist is washed away by the involved water in cutting procedure. Second, the procedure of cleaning chips after cutting and breaking is used with acetone and isopropanol (IPA). It should be noted that the holding position can affect the cleaning outcome. Holding with vertical position can help reduce the probability of particle left. Third, it is difficult to clean the particle left on the reuse substrate.

When solving the particle issue in cleaning procedure thereby avoiding short circuit, the sample with down to 100nm thickness can work as a capacitor.

The fabrication process of the device can be illustrated by following steps: (1) Clean procedure to remove photoresist and particles with acetone and isopropanol (IPA), with is cause by the dicing process and then blow dry with nitrogen. (2) Deposition of 30nm gold layer as bottom electrode by e-beam evaporation followed by 5nm titanium (Ti), act as a stick layer when the substrate shows a clean surface with no particle remaining under optical microscope. (3) Spin coating of PMMA layer. The thickness and uniformity need to be checked by ellipsometer. The thickness investigated includes 100nm, 150nm, 200nm, 300nm and 400nm. (4) Deposition silver top electrode with Edwards Auto500 thin film deposition system via attached shadow mask. Figure 4.2 show the image of final chip to investigate break down voltage.

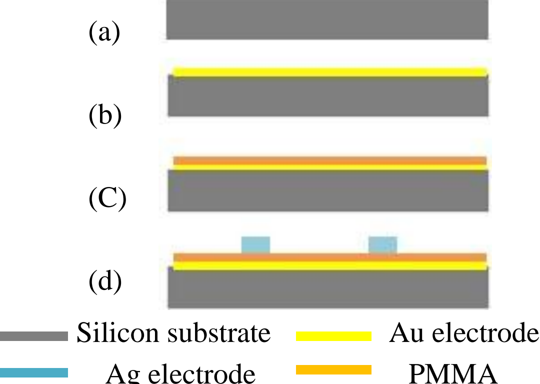


Figure 4.1. The fabrication process of the investigating breakdown voltage device :(a) silicon chip prepared; (b)Au deposition; (2) PMMA Spin coating; (3) Ag deposition. Color indication: Gray: silicon substrate. Yellow: Au layer. Orange: dielectric layer. Blue: Ag electrode.

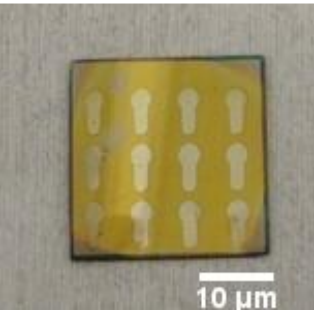


Figure 4.2 image of break down voltage experiment sample.

4.1.3 Characterization and Results

The whole measurement of I-V curve is conducted with probe station, the details of the measurement setup is illustrated in chapter 5. The sample connected to the system by the probes touching the electrodes. Since the bottom one is isolated by PMMA layer, a corner area need to scratch and remove PMMA.

The breakdown voltage measurement is based on the sample of thickness ranging from 100nm to 400nm. Among all the samples with different thickness, 60V is investigated first. For all the five thickness, the dielectrics work. Reaching further to 70V, the sample of 100nm begins to loss its insulating property and the other samples with thickness larger than 100nm they are still insulating. It is obvious to see the current jumps to high value in a sudden at around 65V voltage from the curve showing the damage sample of 100nm. It means that the breakdown voltage of 100nm thickness PMMA layer is around 65V, shown in figure 4.3.

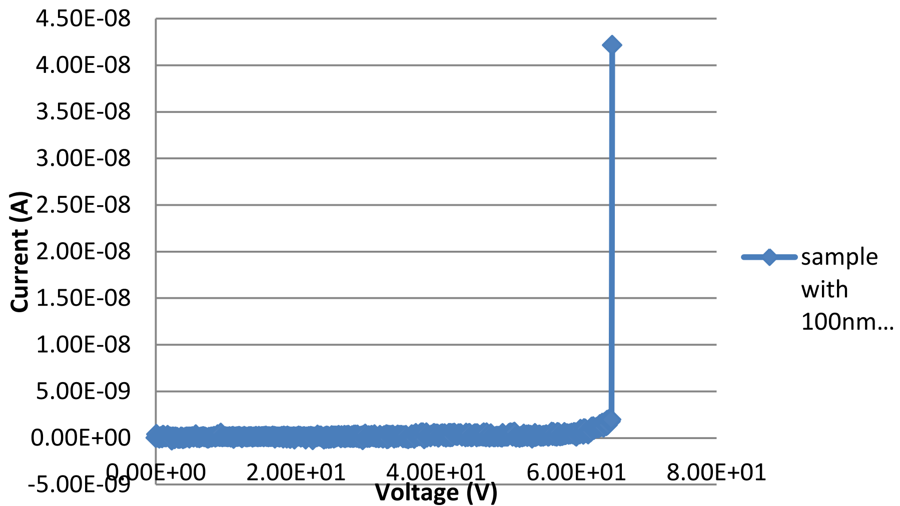


Figure 4.3. Current-voltage characteristics based on the sample of 100nm thickness sweeping from 0 to 70V

However, when the applied voltage is up to 80V, the other four thicknesses from 150nm to 400nm can still work as the dielectrics. Taking the sample of 400nm as an example, which is the thickness used to fabricate the OLETs. The measurement is conducted by sweeping from 0V to 80V and then reverse back to 0V.

According to the equation, when sweeping from 0 to 80V, the voltage sweeping rate $\frac{\Delta U}{\Delta t}$ is a positive fixed value, while the backward sweeping, it is a negative value. And it means the forward sweeping leading to a positive constant current, forming a straight line paralleled to the x-axis. In contrast, the backward sweeping results to a negative constant current. Together with the forward and backward, the I-V curve should show the rectangle shape, which is the same with the curve measured.

Figure 4.4 shows the current-voltage characteristics of the case of sample with 400nm PMMA, indicating the sample can withstand 80V and remaining insulating property at this voltage. The leakage current can be read as around $4*10^{-13}$A. Based on the parameter of this sample, the value is also calculated from equation as $7.74 \times 10^{-12} A$, which is closed to the measured value.

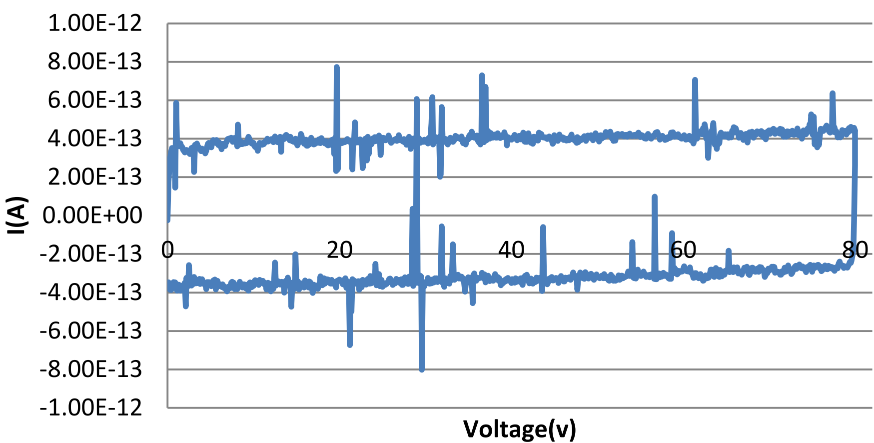


Figure 4.4. Current-voltage characteristics based on the sample of 400nm thickness sweeping from 0 to 80V then back to 0V

Based on all the samples, the results of breakdown measurement is summarized by the table 4.4, it indicates that the 100nm thickness PMMA layer break down when the voltage applies up to 70V and thickness of more than or equal to 150nm, the dielectric still shows insulating property.

Thickness	60V	70V	80V
100nm	√	x	x
Larger than 150nm	√	√	√

Table 4.4. Summary of the breakdown voltage based on the samples with thickness range from 100nm to 400nm

4.2 Stencil lithography

Taking account to the polymer dielectric material, the fabrication recipe of the OFET device with PMMA layer has to do some adjustments comparing the recipe with silicon dioxide layer as dielectric. Here we have to introduce another pattern transfer technique, using stencil lithography instead of lift-off process to pattern structures.

Stencil lithography works as an alternative method of photolithography process. The fabricating process of SiO2 OFET is known as using lift-off process to create the rough and fine source and drain electrode, detail process is shown in figure 4.5. Lift-off process give an inverse pattern by spin coating photoresist first on the substrate surface, then etching produce the openings so that material can be deposit through them. Here the target material covers the whole substrate, including the etched regions and the top of the photoresist regions. When the substrate rinse in the acetone bath, not only the photoresist is removed, but also the material on the photoresist layer is lifted off and wash away. Finally, the substrate only has the target material that directly contacted remains. Since the final step will involve acetone, which reacts

with PMMA, leading to destroy PMMA layer. That is the reason an alternative method should be introduced. Stencil lithography is a simple, low-cost way to patterning without photolithography step and can reach the scale of lift-off process (typically micrometric dimensions). Moreover, Stencil lithography can give the defining submicron scale, single-layer pattern in a simple and ultra-clean way via evaporation method.

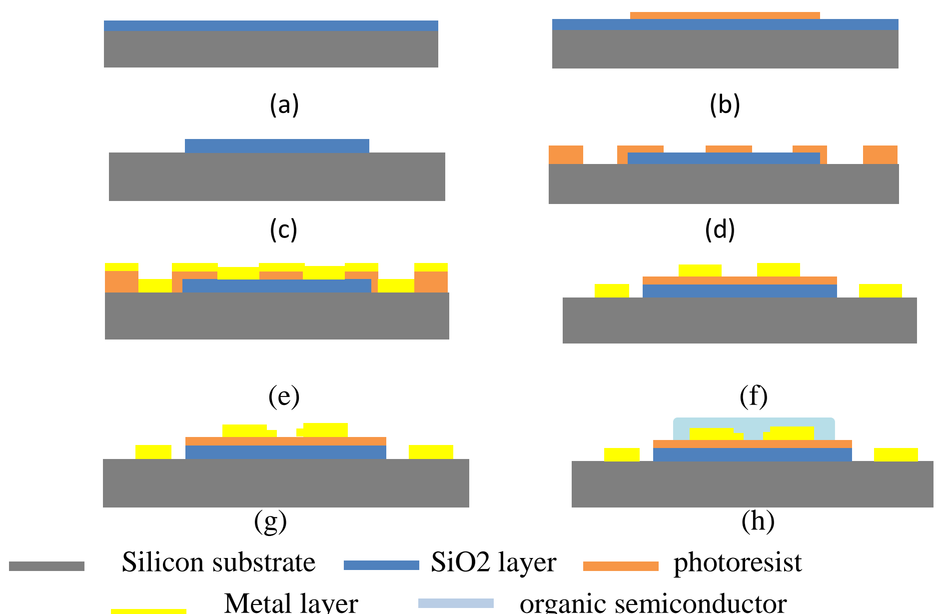
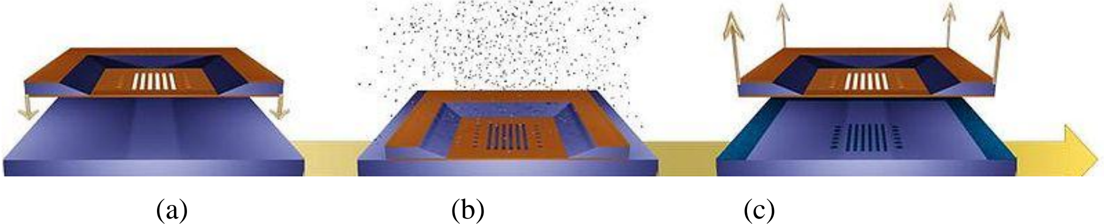


Figure 4.5. Simplified schematic illustration of the fabrication process for an BC/BG configuration OFET device with SiO_2 as gate dielectric: (a) substrate preparation with SiO_2 layer; (b) first photolithography process pattern the photoresist layer; (c) etching SiO_2 layer and removal photoresist; (d) second photolithography process pattern photoresist layer; (e) deposition metal over the substrate; (f) lift-off process to create rough electrode (using the ultra-sonic clean in acetone); (g) third photolithography, second metal deposition and lift off process to create fine electrode; (h) organic semiconductor layer deposition. Color indication: Gray: silicon substrate. Dark blue: SiO_2 layer. Light blue: organic semiconducting layer. Orange: photoresist layer. Yellow: metal layer

The main principle can be illustrated by the Figure 4.6. This technique relies on a shadow mask to let deposition materials pass through and then offers desired pattern. The first stencil was demonstrated by S. Gray and P. K. Weimer in 1959.[33] they deposited metal material utilized long stretched metallic wires shadow mask. With the developing of this technique, now the aperture scale has been down to submicron, which is called a nanostencil. It can be fabricated by various methods, like electron beam lithography (EBL), focused ion beam lithography (FIB) and so on.

It also should be noted that there are still some challenges in the stencil lithography. One of them is aperture clogging. When materials pass through the stencil the deposition material not only stays on the substrate faced to the stencil aperture but also remains aperture inside and around. This effect will reduce the effective aperture size and further result in closing the aperture completely. The other challenge is blurring, which will enlarge the initial pattern and

gap between substrate and stencil. There are deposition material accumulated on the stencil membrane leading to high in-plane residual stresses and further results to membrane deformation. And the stress is mainly caused by material diffusion on the substrate and the geometrical setup of the evaporation. One of the solutions was reported by Marc A.F. van den Boogaart.[34] According to the deposition-induced stress theory mention earlier, they use both normal stencil and corrugated structures to deposition chromium on the substrate and investigate how the burring and clogging phenomena effect. It shows corrugated-structure stencil can be used to reduce the membrane deformation and control the surface pattern.



(a) (b) (c)

Figure 4.6. Schematic diagram of the stencil lithography process: (a) alignment of stencil with substrate. (b) Deposition materials through stencil. (c) Separation of stencil and substrate,

The stencil design is based on the design of the OFET substrates. The final design of OFET device is shown in figure 4.8. It requires both rough and fine electrodes working as source and drain. The dimension of rough electrode needs to be measured with scanning electron microscope (SEM), from which the actual dimension can be obtained. The average distance from side shorter electrode to the edge is 1.57μm and the average distance between source and drain electrode is 523nm.

It requires two masks to fabrication the stencil. One is for the back-side open window; the other is for the front-side aperture. The whole design is completed via L-edit, which is a software producing layout.

The mask for stencil to create the fine source and drain electrode is designed as 9 different dimensions by varying the value of m and n, where m refers to the overlap distance of the two electrodes and n is the distance between the two electrodes. The distance of m and n corresponds to the channel width and channel length in OFET devices. The designed m value refers to 100, 200 and 300μm and designed n value is 5, 10 and 25μm, they provide 9 different electrode mask, shown in figure 4.8.

The design of the mask for window can be illustrated in figure 4.8. The dash rectangle is the window mask opening and orange one refers to the membrane area. The dash line is determined by the inside orange rectangle via the etching process. As silicon is single-crystal material, the etching rate depends on the crystal face, resulting in high anisotropy. Aqueous caustics can be the wet etchants, and potassium hydroxide (KOH) is used here. It displays the etch rate of (100) plane is 100μm per hour and (111) plane is 1μm per hour, this high etch rate selectivity contributes to a trapezoidal shape cross-section. Silicon etching is illustrated in figure 4.7. Since the angle between (111) plane and (100) plane is 54.7˚,

$$x = \frac{d}{\tan 54.74^{\circ}}$$ (Equation 4.6)

Where x is the distance of the slope shadow-casting onto plane (100) and d is the wafer thickness, known as 525µm. therefore, x can be easy obtained by the equation, that is, 371.17µm

Moreover, the dimension relation between the window opening, referring the dash rectangle and the membrane referring the orange rectangle follows:

$$a = u + 2x$$ (Equation 4.7)

$$b = w + 2x$$ (Equation 4.8)

where a is the width of window mask, b is the length of window mask, u is the width of membrane and w is length of membrane.

Accordingly, a and b can be calculated according to the relation, and the dimension of the inside rectangle is 1550µm*100µm.

$$a = 100 + 2 \times 371.17\mu m = 842.34\mu m$$ (Equation 4.9)

$$b = 1550 + 2 \times 371.17\mu m = 2292.34\mu m$$ (Equation 4.10)

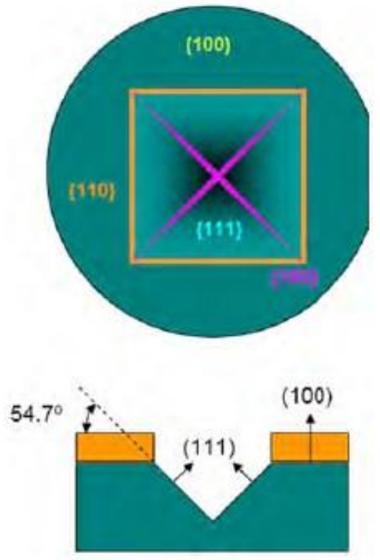


Figure 4.7.illustration of silicon etching

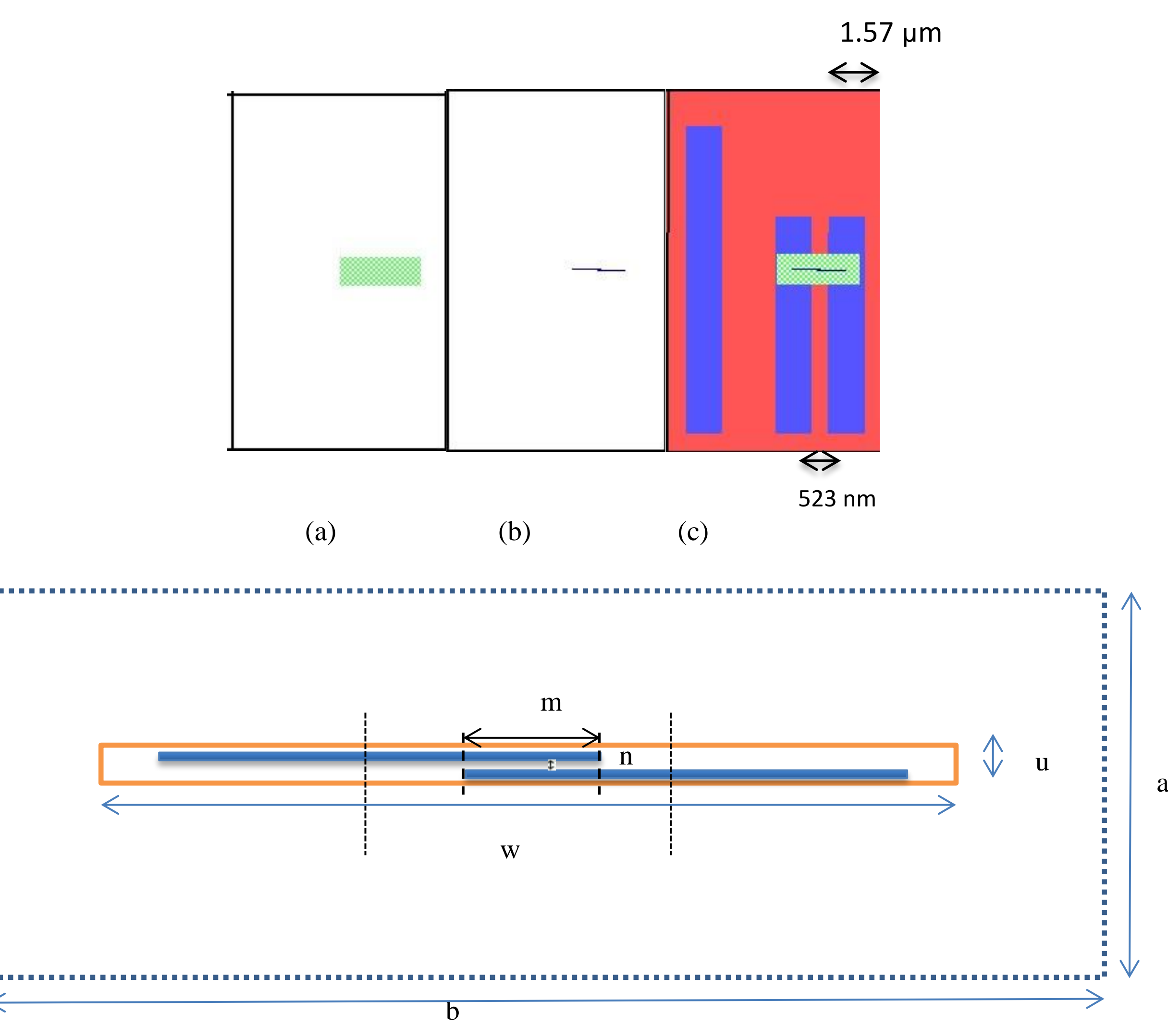


Figure 4.8. the design of masks. (a) The mask of back-side drawn by L-edit; (b) the mask for opening on the front-side drawn by L- edit; (c) designed stencil align with the final device; (d) the detail design dimension of the masks

With prepared mask, the stencil can start to be fabricated. The process step is detailed is shown in figure 4.9. The nanostencils were prepared from a 525 μm thickness 100μm diameter silicon wafer with 300 nm low-stress silicon nitride (SiN) layer. The font SiN layer is patterned by photolithography and reactive ion etching, and the back membrane is created by photolithography, reactive ion etching and KOH etching. The front-side photolithography includes HMDS, spin coating photoresist with 1.5 μm, baking 90 ℃ for 60 s exposure 1min 45s with the mask shown in Figure 4.8 (b), Developing in AZ 351B (mix with DI water, ratio 1:4), for 60 s, agitation, rinse in water (fine rinse bath) for 2 min and spin dry. Front-side reactive ion etching uses SF6 30sccm 1500sp for 1min45s. There are several adjustments of back-side photolithography. The exposure time is increased to 5s with the mask shown in Figure 4.8 (a). Dry etching time prolong to 6 min. KOH etching uses 8wt% KOH concentrations at 80 ℃ for approximate 9 hours.

During the fabricating process, several parameters should be investigated. First, the exposure time of front-side wafer to create electrode pair. In order to obtain a well-patterned electrode pair, a test wafer is exposed with 4.0s, 4.3s, 4.6s and 4.9s thereby determining 4.3s as the exposure time.

Second, etching time on the front side to create fine electrodes is one of crucial parameters. Test experiments are conducted from 1.5min to 4.5 min. For the stencil with 4.5min, the fine electrodes are over etched and exhibit a curve shape, which makes the OFET device hard to characterize with the irregular-shape source and drain electrode. For the stencil with lower etching time, the electrodes are not completely form with a not etch through aperture. And based on the test experiments, the final stencil used is etched 3min.

Third, since the etching time to create the back-side window with KOH solution is a calculated value, the thickness requires to be checked in the meantime.

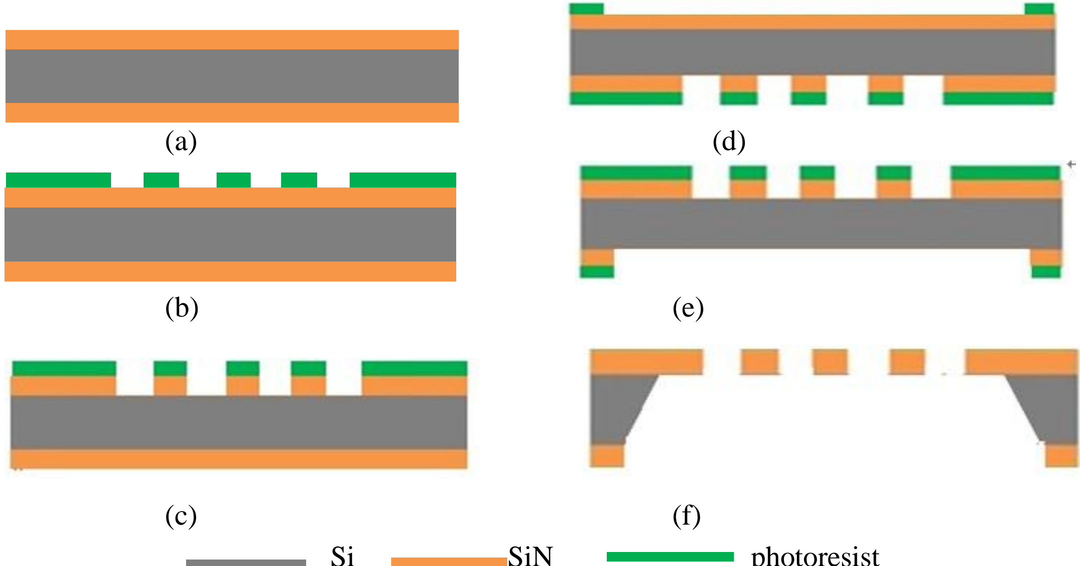


Figure 4.9. Simplified schematic illustration of the fabrication process for a stencil: (a) Si wafer with 300nm SIN; (b) photolithography definition on front side structure; (c) ICP-RIE etching on front side; (d) photolithography on back side structure; (e) etching on back side structure; (f) KOH etching. Color indication: Gray: silicon substrate. Orange: SiN layer. Green: metal layer.

Then the rinse and gentle blowing wafer needs to cut into 6*10μm chips which requires photoresist coated. In order to conduct the coating procedure, a slice of flat blue tape needs to cover the wafer then the wafer can be sucked by the machine. Finally the chip is cleaned with acetone, isopropanol (IPA), deionized (DI) water, and then blowing dry gently. During the process, the wafer should be taken extremely careful due to the wafer after KOH is super fragile. Figure 4.11 shows the final stencil and electrode deposited on a substrate using stencil. They are both taken under optical microscope.

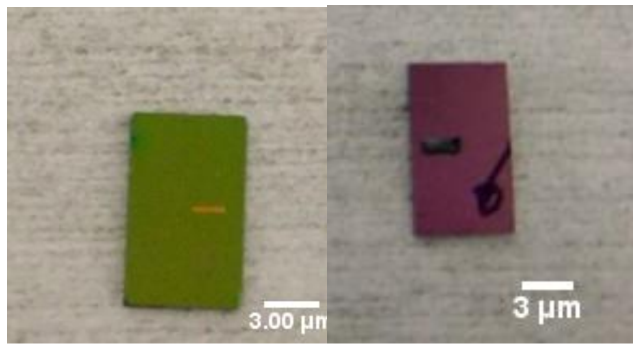
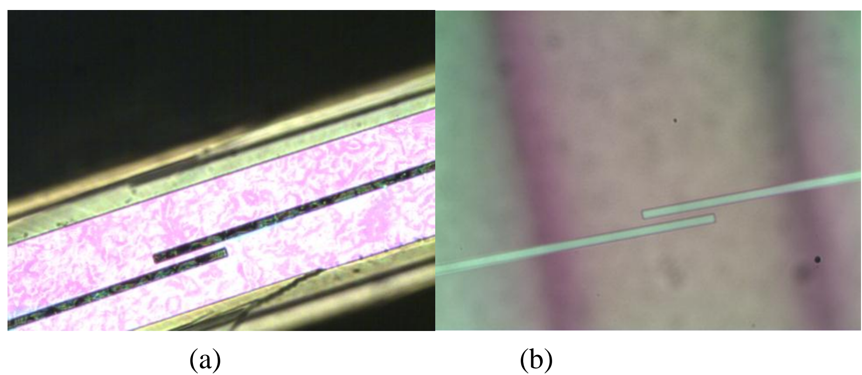


Figure 4.10 image of front-side (left) and back-side (right) stencil



(a) (b)

Figure 4.11. Optical microscope images under 20 times magnitude (a) stencil with dimension of 10μm length and 100μmwidth. (b) Fine electrodes deposited through the stencil.

4.3 Fabrication of OFET device

The OFET is based on the wafer of 100 µm diameter, 400 µm thickness and B-doped silicon wafer. The wafer need to dice to small chips, which is 6 µm*10 µm designed in this project. In order to reduce particles that the dicing procedure cause left on the chip, we need to spin coat photoresist first to protect the wafer and do HMDS to stick the photoresist. Then the wafer can be taken to the dicing room. The dicing saw equipment is Disco DAD-2H5. The wafer should have 150 µm height left and breaks manually in the cleanroom.

The following fabricating procedure is conducted in the cleanroom, which is humidity and temperature controlled. Cleaning procedure plays an important role in this whole fabrication to avoid particle left on the substrate surface, which can cause short circuit in later electrical measurement. Based on different conducted cleaning methods, I choose to clean with acetone under ultrasonic agitation in a vertical position then flow acetone and IPA on the substrate, rinse in DI water, blow dry and finally make sure a clean surface with no remaining under microscope.

With a clean Si chip, organic field effect transistor is fabricated based on BC/BG and TC/BG configurations, various sizes of stencil, gold and aluminum electrodes. As to BC/BG configuration, the fabrication process can be simplified illustrated in figure 4.11.

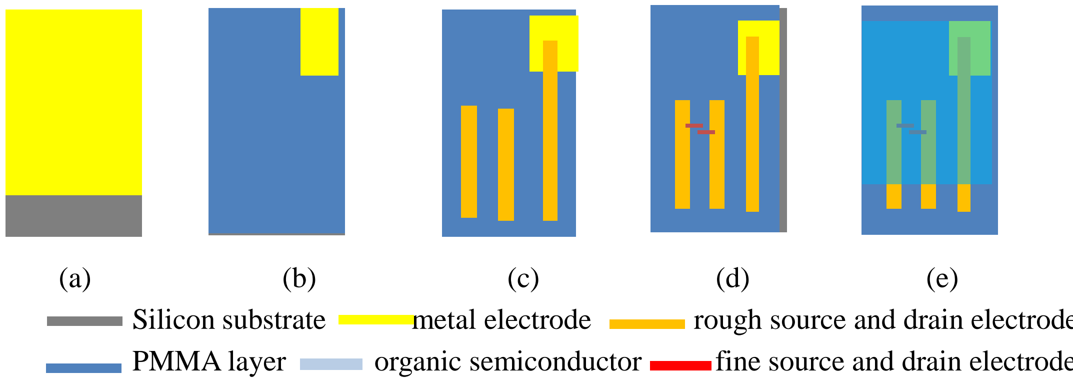


Figure 4.12. Simplified schematic illustration of the fabrication process for a BC/BG configuration OFETs: (a)bottom gate deposition blank with slice space; (b) PMMA coating removing the corner area; (c)big electrode deposition with shadow mask; (d) small electrode deposition with stencil; (e) PPTTPP thin film deposition. Color indication: Gray: silicon substrate. Dark blue: SiO2 layer. Light blue: organic semiconducting layer. Orange: photoresist layer. Yellow: metal layer

As to BC/BG configuration, the first step is deposition 5nm titanium (Ti) and 30nm gold (Au) layer by e-beam evaporation with a slice of bottom space covering with foil to have the rectangle area exposed to silicon. The Cryofox Explorer 600 is used for realizing the uniform bilayer. The deposition parameters need to set first, including the thickness, rate, base pressure etc. The sample is placed in a 10*10μm holder. The sample holder is selected based on the sample size and shape. The deposition details can be found in Appendix D.

Next, dialectic layer PMMA is coated with 500rmp for 5s and followed by a higher rotation of 4000rpm for 45s to achieve a uniform layer of 400nm PMMA, then the substrate is removed with right corner part of PMMA by acetone according to the rough electrode shadow mask. Next, the prebake procedure is taken place at 200℃ for 1 min on hot plate. This process can remove the remaining solvent from the PMMA. Noted that the interval between the end of spin coating and the beginning of baking should be minimized,[30] for the purpose that avoid aggregation of the solution and forming droplets thereby degrading the uniformity of PMMA layer thickness. Furthermore, the thickness needs to be checked through the ellipsometer.

Deposition 30 nm source, drain and gate electrode with shadow mask, shown in Figure 4.13, which contains two same shorter length rectangle openings and one longer length rectangle opening. Both Au and Al layer are investigated as electrode material. The process is conducted by e- beam evaporation using Cryofox in the cleanroom. When aligning the shadow mask with the substrate should make sure the longest opening is at the same position with the corner part without PMMA, by means of which the longest electrode through shadow mask can touch the bottom gold layer, working as gate electrode. Meantime, part of the two electrodes touch silicon, where is the area for connecting the measurement probe.

Figure 4.13. The shadow mask drawn by L-edit

It is noteworthy that substrate should be checked via microscope after each step to make sure the sample in good status. The undesirable status can be caused by the following respect. First, the unsatisfactory layer deposition. For example, the edge of rough electrode touches the bottom gold layer. Second, particle involved in fabrication process. The possible particle can be introduced by the cleaning procedure after cutting, unclean rough shadow mask, pipes used for PMMA. Third, distortion stencils result to the fine electrode touched or deformed. These circumstances need to be examined not only with optical microscope but also with short circuit experiment. Considering most of the possibity are involved before stenciling, the short circuit experiment is conducted before the stencil lithography. Short circuit measurement is conducted on the platform of probe station. The platform detail will be illustrated in the electrical measurement section. And later the condition of fine electrode pair can be checked under microscope.

Then using stencil to create fine source and drain electrode pairs. The holder with alignment stencil and substrate is shown in figure 4.14. The alignment is conducted based on the holder under optical microscope. With black tape which is used for vacuum deposition fixing the substrate, the stencil aligns the aperture with the gap between rough source and drain, shown in figure 4.14. The window side of stencil is facing the optical lens. And with foil strip the stencil bonds with substrate.

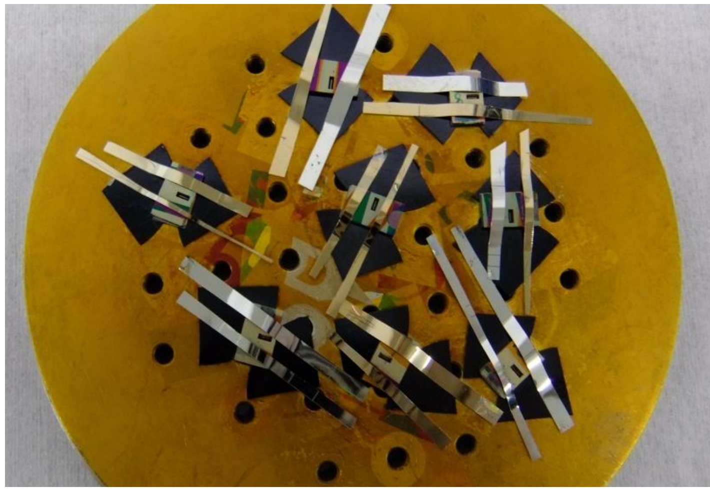


Figure 4.14. Image of the alignment holder with substrate and stencil

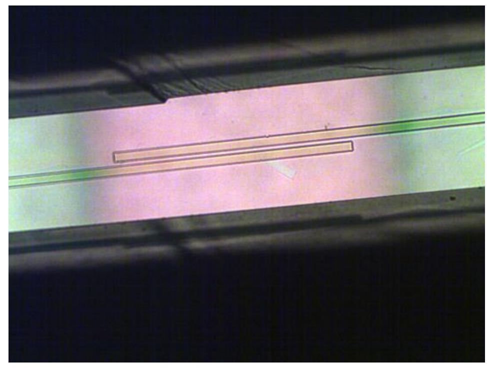
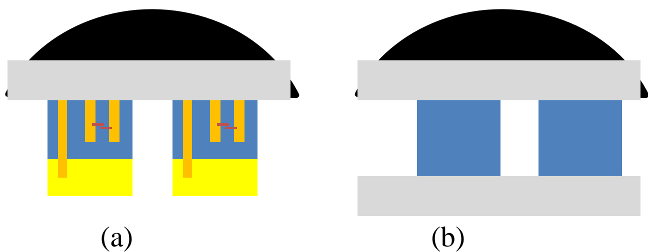


Figure 4.15.optical microscope image of alignment under 20 times magnitude

Finally, depositing organic material in MBE vacuum chamber, which is PPTTPP thin film in this project. The sample fabricated need to fix on the holder in the way shown in the Figure 4.16(a), covering the bottom side of the sample, which is used for the electrical measurement. It also should be noticed that the sample is not supposed to exposure with ambient air too long time. Simplified procedure of growing PPTTPP thin film can be demonstrated into the following steps with initial condition that the chamber is pumped down: (1) disconnect the transfer chamber from the rough pump; (2) Turn off the turbo pump; (3) Waiting 20-30 min, connect nitrogen to the chamber; (3) disconnect nitrogen after the chamber has been vented; (4) mount the sample holder; (5) pump down the chamber and increase oven temperature to 390 ℃ by turn on the power supplies; (6) waiting the pressure reaches lower 10^{-4}mbar, start to deposition by open the shutter with deposition rate around 0,2-0,3 Å/sec and stop the deposition when the thickness reaches 30nm; (7) ventilate the chamber and take out the sample holder; (8)pump down the chamber. The experiment details can be found in Appendix D.

Figure4.17 show a final OFET device based on BC/BG configuration, gold electrode, PMMA working as dielectrics, which is ready for electrical measurement.



(a) (b)

Figure 4.16. Chip arrangement of sample holder. (a) with BC/BG configuration; (b) TC/BG configuration

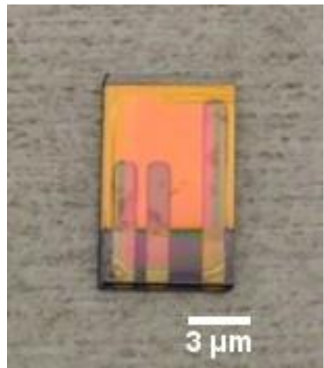


Figure 4.17 image of OFET devices

For TC/BG configuration, in the beginning two steps the procedure is same with BC/BG, depositing titanium and gold, coating PMMA layer. Then the sample is put into MBE chamber having PPTTPP thin film, fixing based on the way shown in Figure 4.16 (b). Finally, the sample is taken back to cleanroom having source drain electrode pairs. The main purpose of the device design is for probe connecting in electrical measurement and Figure 5.2 shows the connecting way. The alignment of the stencil to the device substrate is done manually under a white light microscope.

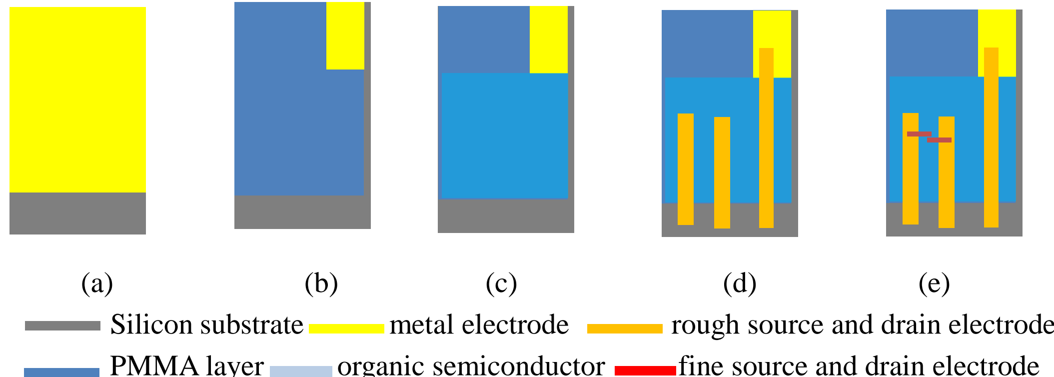


Figure 4.18. Simplified schematic illustration of the fabrication process for a TC/BG configuration OFETs: (a)bottom gate deposition blank with slice space; (b) PMMA coating removing the corner area; (c) PPTTPP thin film deposition; (d) big electrode deposition with shadow mask; (e) small electrode deposition with stencil;

CHAPTER 5 ELECTRICAL EXPERIMENTS (I – V MEASUREMENTS)

The electrical experiment in this chapter is mainly carried to obtain transfer characteristics (drain current versus gate voltage at constant source-drain voltage) and output characteristics (drain current versus source-drain voltage at constant gate voltage), and then extract the mobility and threshold voltage thereby investigating the function of configuration, channel length, gate material, electrode material in the performance of OFET devices.

5.1 Experimental setup

The electrical measurement platform consists of a Stanford Research SR570 current pre-amplifier, a 16-bit National Instruments DAQ card, Falco system WMA-02 and WMA-280 DC voltage amplifier and three probers, which is illustrated in Figure 5.1. Sample is connected by source, drain and gate electrode. The source get the input signal from SR70 current pre-amplifier, which is grounded, the drain and gate are connected with the output of DC voltage amplifier with 20 times signal multiplier. Then the signal is gathered by DAQ device adaptor, and finally sent to DAQ card, which can only provide maximum 10 volt. The measurement is under room temperature and inside "black box" to reduce noise around and less movement of surroundings is preferred. The connecting between probe and sample is shown in figure 5.2

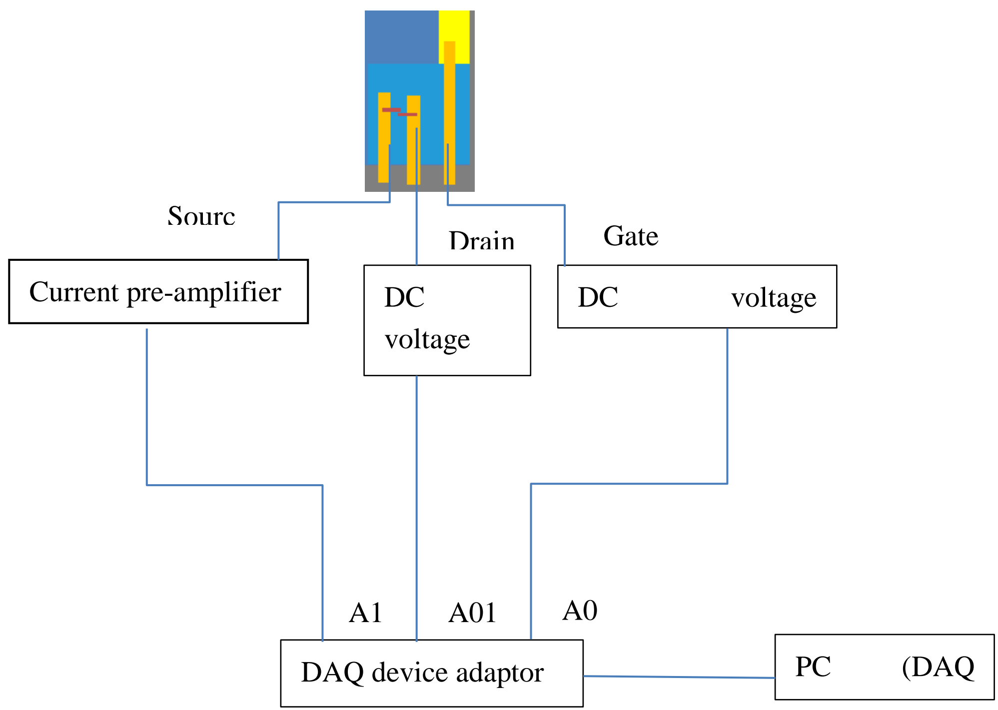
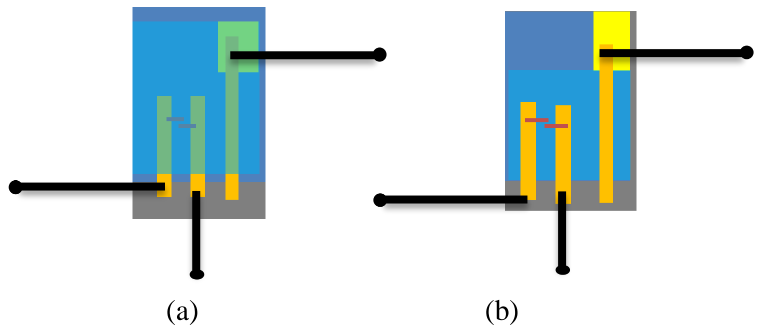


Figure 5.1.Schematic diagram of electrical measurement setup



(a) (b)

Figure 5.2. Way of OFET connecting to probes with. (a) BC/BG conguration; (b) TC/BG configuration

5.2. Current-voltage characteristics

Short circuit measurement is first conducted based on the platform of probe station. The sample measured here is based on BC/BG configuration and without fine electrodes and PPTTPP thin film layer,

To put it simple, the substrate, shown in Figure 4.13 is connected with the corresponding probes and the voltage setting has to below the breakdown voltage of PMMA. When sweeping with source-drain voltage, the source-drain current Ids flow around zero. While when sweeping with the gate voltage, source-drain current flows a “rectangle-shape” curve. These curves show the same trend as I expect, meaning the dielectric works well as insulator. Then after the rest deposition finished, the sample can start to measure its OFET properties.

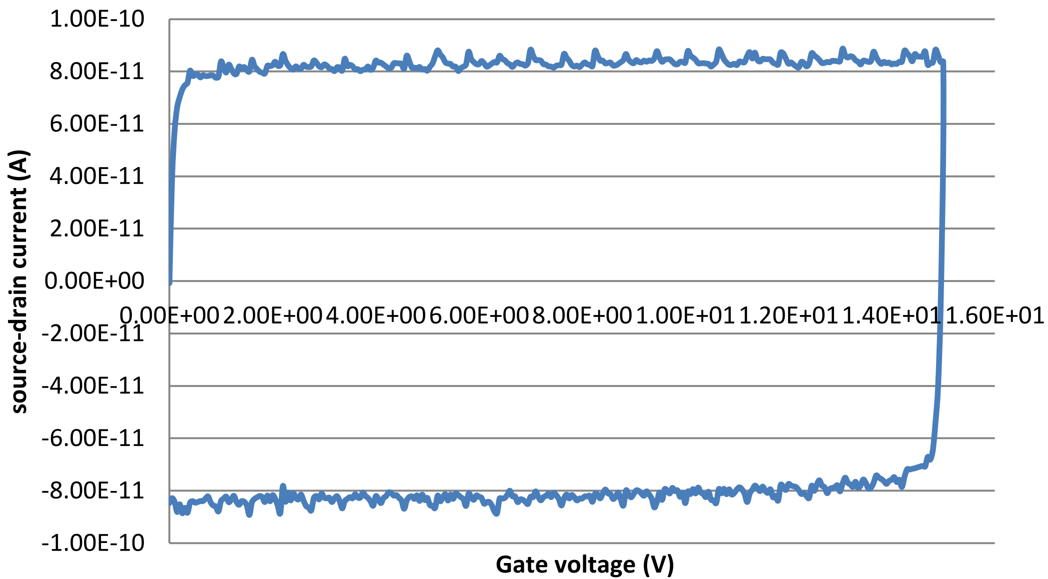


Figure 5.3. Current-voltage characteristics of the sample before stencil lithography

Based on that, the measurements to investigate the electrical feature of OFET device can be

conducted in two different ways, one sweeping gate voltage for different constant source-drain voltage called transfer characteristics, the other sweeping source-drain voltage for different constant gate voltage called output characteristics. Considering the breakdown voltage of PMMA, the output characteristics sweeping program setting illustrates as follows: sweeping source-drain voltage from 0 to -60V and then back to 0V at constant gate voltage and the constant chosen as 0V, -10V, -20V, -30V, -40V, -50V, -60V. The delay time between every change sets as 10 second, which is used to avoid a transient behavior. The positive sweeping and transfer characteristics sets as the corresponding way.

Taking the group of samples based on TC/BG configuration with 10 μm channel length and 100 μm channel width as an example. Figure 5.3 shows the output characteristic sweeping both positive and negative direction. And figure 5.4 shows and the corresponding transfer curve in negative direction. The output characteristics measurement is conducted by sweeping from 0 decrease to -60V, then from 0 towards 60V. It shows evident properties of p-channel OFETs. The holes work as the majority charge carriers in in both positive sweeping and negative sweeping, which accumulate and form the current from drain to source. For negative half, holes are accumulated to form evident linear and saturation regime and the source-drain current increase with the gate voltage. While in positive half, holes rejected with increasing positive gate voltage and the current in an inverse proportion to the gate voltage

From the output curves in negative direction, linear regime and saturation regime can be easily observed. When looking at single curve at constant V_g, the current starts from approximate zero ampere with no source-drain voltage applying and current begin to flows with a bias applying, which shows linear proportion to V_{ds} and then increases to a horizon line at high V_{ds}, that is, saturation regime. Furthermore, the drain current increase with gate voltage, which means a large density of charge carriers accumulated with high gate voltage. This tendency can be proven by the transfer curve. The orange curve refers to -50V source-drain voltage applying. The current in this curve increases with gate voltage, reaching at $-9*10^{-8}$ A at Vg = -60V, which is the same value read from output characteristics

Focusing on the red curve in output characteristics, the drain current is around zero when source-drain voltage sweeps from 0V to -60V, meaning no or very small leakage current flows. While as to the case with no source-drain voltage, it can be read that the current in the output light red curve is$-6.56*10^{-9}$ A and it matches with the corresponding value shown in transfer dark blue curve is $-7.49*10^{-9}$ A. It means the leakage current appears at high gate voltage and the value is around this order. The reported leakage current based on self-assembled monolayers (SAMs) [3] or cross-linked polymer [19] exhibits on the order of 10^{-8} A, which implies good performance of PMMA gate dielectric. The results also indicate the performance of the device can be trusted.

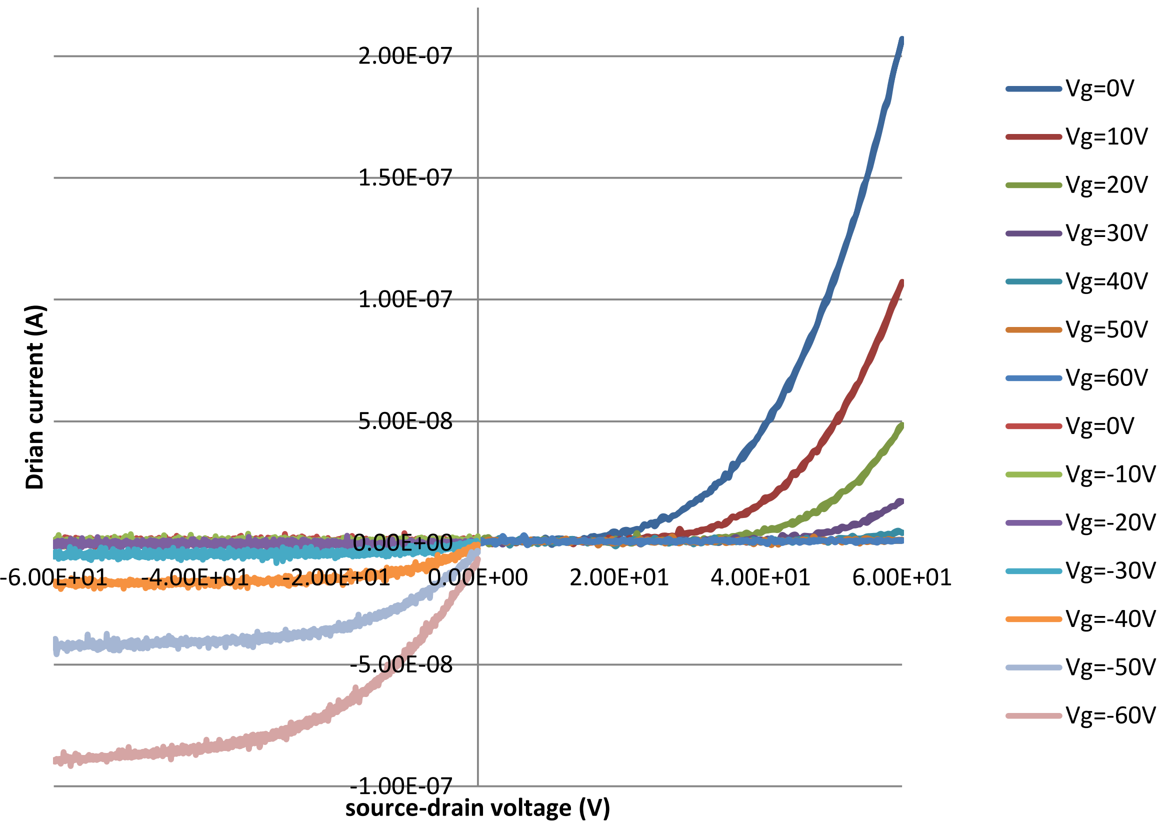


Figure 5.4. Output characteristic with Vg from -60V to 60V based on the group of top contact bottom (TC/BG) configuration with length L=10 μm and width W=100 μm

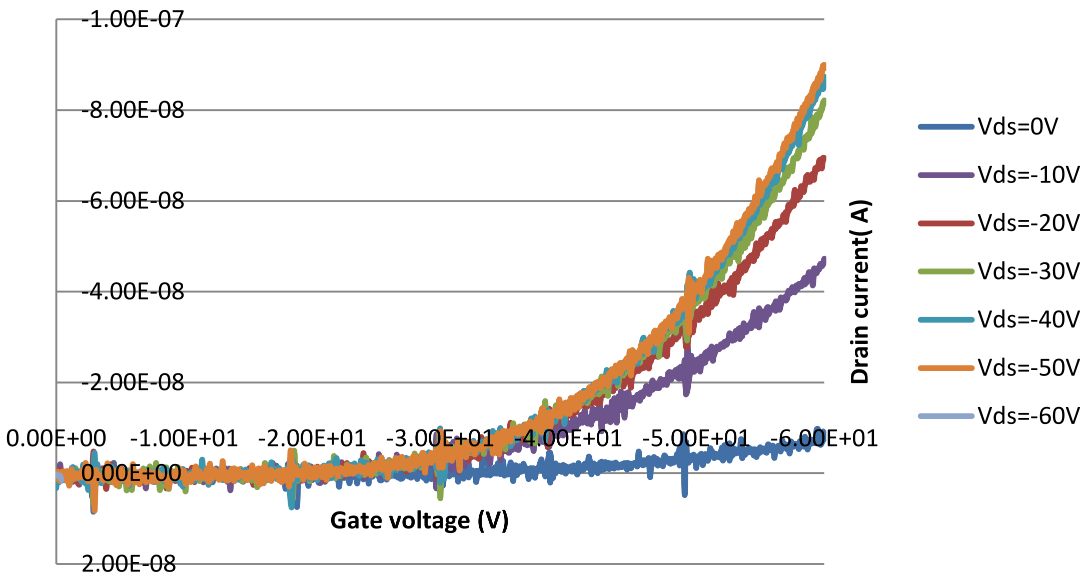


Figure 5.5. Transfer characteristic sweeping Vg from 0V to -60V based on the group of top contact bottom (TC/BG) configuration with length L=100 μm and width W=10 μm

.

5.2.1 Configuration dependence

The measurement is conducted based on OFET device with BC/BG configuration and device with TC/BG configuration. Both device uses PMMA as gate dielectrics and 10 μm channel length, 100μm channel width.

Figure 5.5 shows current versus drain-source voltage curve at zero gate voltage based on BC/BG (blue curve) and TC/BG (red curve) configurations. It is plotted in different current scale to show the tendency of the two conditions clearly. Apparently, BC/BG configuration exhibits lower output than the TC/BG configuration. The maximum current of bottom contact and top contact one differ by two orders of magnitude. It can be illustrated by the charge carries injection region of the two configurations, leading to a high contact resistance associated with the high injection barrier to the organic material of the bottom contact device.[4]

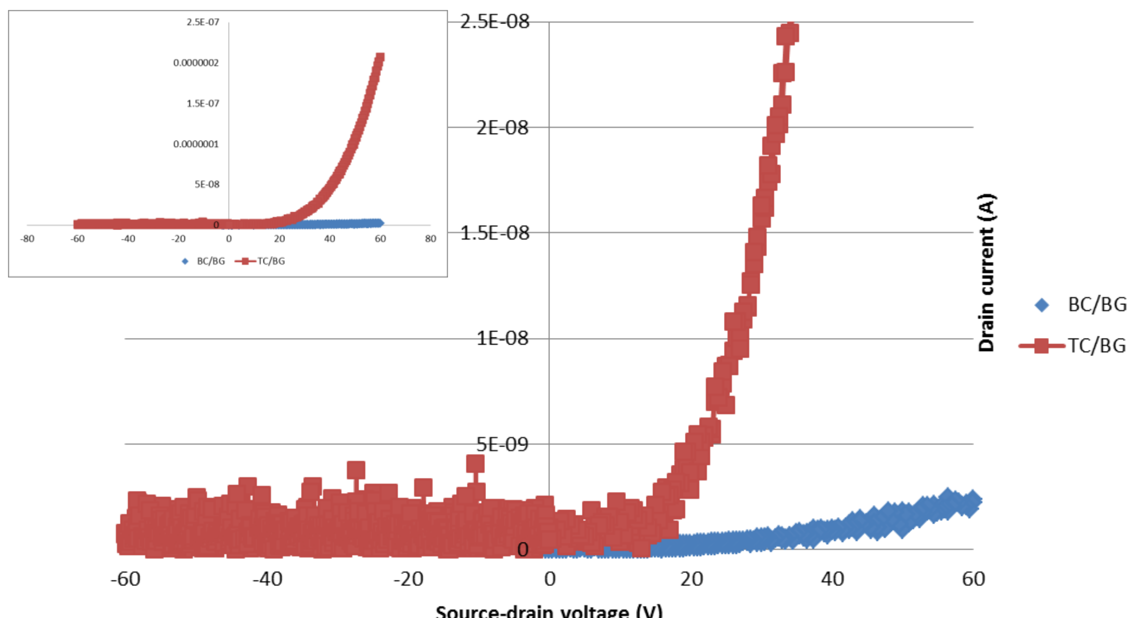


Figure 5.5. Output characteristic at Vg =0V with 10 μm channel length and 100 μm channel width group based on TC/BG and BC/BG configuration in two different scale

According to the equation, the mobility of holes can be calculated as follows and the parameters can be obtained by our design.

$$\mu_{lin} = \frac{\partial I_d}{\partial V_g}\Big|_{V_{ds}=-10V} \cdot \frac{L}{W \cdot C_i \cdot V_{ds}} \qquad \text{(Equation 5.1)}$$

Capacitance Ci per unit area can be calculated based on equation, where the distance of dielectrics PMMA is measured by ellipsometer d≈402nm, the dielectric constant of PMMA k≈3.5, the vacuum permittivityε_0= = 8.85 x 10^{-12} (F m^{-1}).

$$C_i = \frac{k\varepsilon_0}{d_{PMMA}} = \frac{3.5 \cdot 8.85 \cdot 10^{-12}}{402 \cdot 10^{-9}} = 7.74 \times 10^{-5}\, F/m^2 \qquad \text{(Equation 5.2)}$$

Here group 1 refers to the sample of bottom contact bottom (BC/BG) configuration with length L=10 μm and width W=100 μm; group 3 refers to the sample of top contact bottom (TC/BG) configuration with length L=10 μm and width W=100 μm;

In the case of group 3, the slope of source drain current to gate voltage can be obtained in transfer characteristics when source-drain voltage is -10V, illustrated in Figure 5.6. The figure 5.6 is plotted by 0 to -50V and -50 to -60V separately to show the linearity of linear regime and the slope coefficient can be read as $2*10^{-9}$A/V.

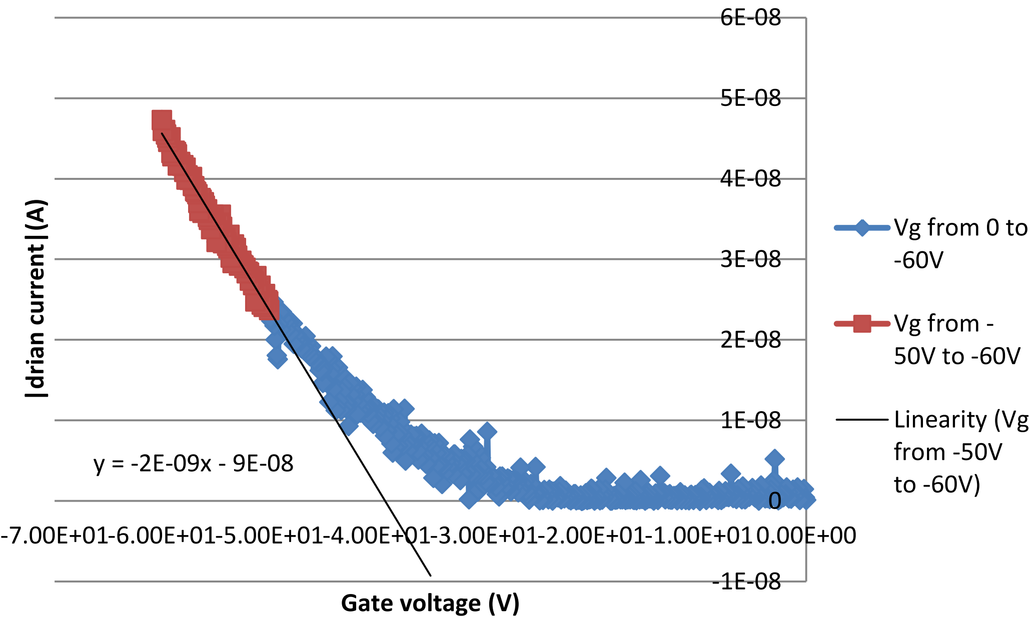


Figure 5.6 Transfer characteristic plotting with sweeping Vg from 0V to -60V and from -50V to -60V separately at Vds = -10V based on the sample of top contact bottom (TC/BG) configuration with length L=10 μm and width W=100 μm

Therefore, the mobility can be obtained

$$\mu_{lin}\Big|_{S_3, V_{ds}=-10V} = 2 \cdot 10^{-9} \cdot \frac{10}{100 \cdot 7.74 \cdot 10^{-5} \cdot 10} = 2.58 \times 10^{-7} (m^2/V \cdot s) = 2.58 \times 10^{-3} (cm^2/V \cdot s)$$

(Equation 5.3)

In the same way, it is easy to obtain the mobility of group1,

$$\mu_{lin}\Big|_{S_1, V_{ds}=-10V} = 3 \cdot 10^{-10} \cdot \frac{25}{100 \cdot 7.74 \cdot 10^{-5} \cdot 10} = 9.69 \times 10^{-8} (m^2/V \cdot s) = 9.69 \times 10^{-4} (cm^2/V \cdot s)$$

(Equation 5.4)

It is obvious that the mobility of top contact bottom gate (TC/BG) configuration is larger than the BC/BG configuration, which means in top contact charges are easier to accumulate.

Threshold voltage also can be obtained from the transfer curve, but it need to plot in a different way with the square root of drain current as the y-axis, which discussed in section 2.2. In this plotting way, there is a linear relation between $\sqrt{I_{d,sat}}$ and gate voltage and threshold voltage can be extracted by an extra linear plotting.

In the case of group 3, which is the top contact bottom gate configuration (TC/BG) with the length L=10 µm, the width W=100 µm. The threshold voltage can be read from the cross- point between the line of linearity tendency and x-axis, which is -28.6V.

As to the configuration, it indicates that the performance of TC/BG configuration is superior to BC/BG, because charges are injected from both the edge and surface of the electrode in top contact device causing low injection resistance.

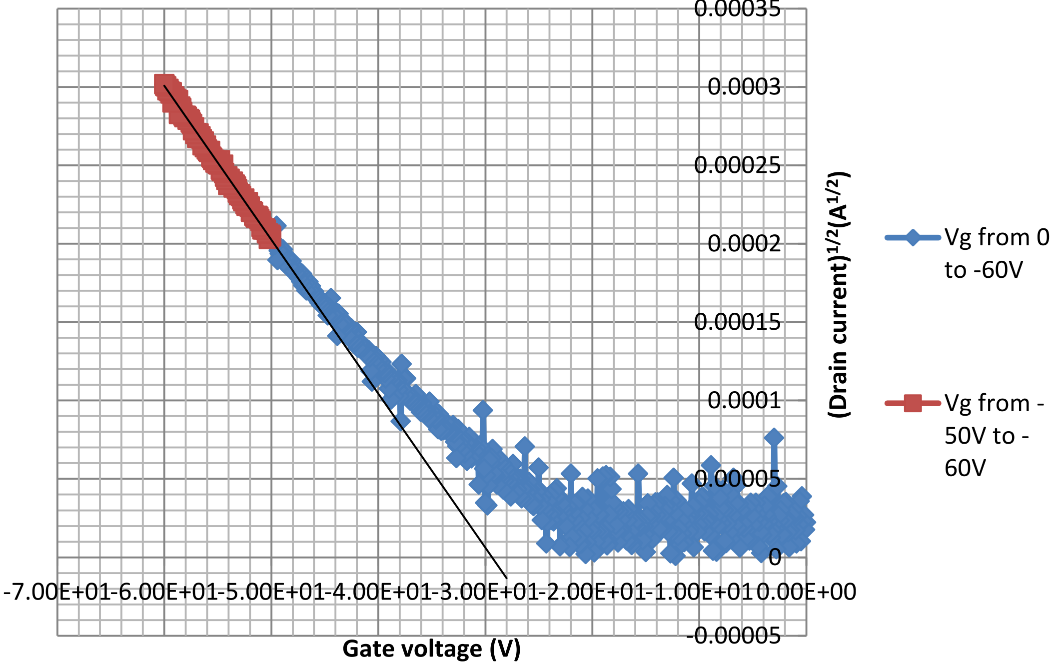


Figure 5.7 Transfer characteristic plotting with Vg from 0V to -60V and from -50V to -60V separately at Vds= -60V based on the group of top contact bottom (TC/BG) configuration with length L=10 µm and width W=100 µm

5.2.2 Channel length dependence

The measurement is conducted based on OFET device with 10 µm channel length and device with 25 µm channel length. Both devices possess TC/BG configuration and PMMA as gate dielectric.

Group 4 refers to the sample of top contact bottom (TC/BG) configuration with length L=25 µm and width W=100 µm.

$$\mu_{lin}\Big|_{S_4,V_{ds}=-10V} = 3\cdot 10^{-9}\cdot\frac{25}{100\cdot 7.74\cdot 10^{-5}\cdot 10} = 9.69\times 10^{-7}(m^2/V\cdot s) = 9.69\times 10^{-3}(cm^2/V\cdot s)$$

(Equation 5.5)

Compare with the mobility calculated based on group 3 with 10μm channel length, group 4 shows lager mobility. The reason can be traced back to equation 2.13, which shows the relation between mobility and channel length. it increases with channel length when other parameters stay in same condition. Hence, the device with 25μm has larger mobility than the one with 10μm

The parameters of all 4 kind groups can be achieved in the same way. Here group 1 refers to the sample of bottom contact bottom (BC/BG) configuration with length L=10 μm and width W=100 μm; group 2 refers to the sample of bottom contact bottom (BC/BG) configuration with length L=25 μm and width W=100 μm; group 3 refers to the sample of top contact bottom (TC/BG) configuration with length L=10 μm and width W=100 μm; group 4 refers to the sample of top contact bottom (TC/BG) configuration with length L=25 μm and width W=100 μm.The calculated mobility and threshold voltage based on these four shows in Table 5.1. It is obvious that the mobility depends on the configuration and channel length and the threshold voltage is mainly differing from the configuration. And the best performance the OFET devices refer s to group 4 based on top contact bottom (TC/BG) configuration with length L=25 μm and width W=100 μm, which is the result as expected.

	Configuration	Width (μm)	Length (μm)	Mobility (cm^2/V^{-1} s^{-1})	Threshold voltage (V)
Group 1	BC/BG	100	10	$9.69*10^{-4}$	-13.3V
Group 2	BC/BG	100	25	$1.29*10^{-4}$	-20V
Group 3	TC/BG	100	10	$2.58*10^{-3}$	-28V
Group 4	TC/BG	100	25	$9.69*10^{-3}$	-28.6V

Table 5.1. Parameters of the four samples measured

Similar experiments have been reported based on pentacene OFET. S.P. Tiwaril et al. utilized a device with 500nm PMMA as a gate dielectric on flexible substrates in top contact configuration. [37]ITO and aluminum acted as gate materials respectively. Their device show mobility up to 0.07 cm2/$V^{-1}s^{-1}$ based on ITO and 0.025 $cm^2/V^{-1}s^{-1}$ based on Al gate material. they believed that the difference is caused by the Al surface roughness is higher than ITO surface and thereby contributing to the contact resistance for the Au S/D on pentacene. Kang et al. presented pentacene OFET using ITO as gate electrode and PMMA as gate dielectric in TC/BG configuration.[38] The authors found the mobility of 0:045 cm^2V^{-1} s^{-1} and threshold voltage of -27.5V. Furthermore, as mentioned in section 2.2.2, J. Puigdollers et al. also fabricated a pentacene thin-film OFET based on PMMA dielectrics. The device shows 0.01 cm^2 $V^{-1}s^{-1}$ mobility and -15 volt threshold voltage.[31]

It can clearly be seen that the reported results and the measured results are in the same order but with some difference. One possibility could be the different organic semiconductor used

resulting in different mobility and threshold voltage ascribed to dielectric/semiconductor interface morphology and carrier trapping sites respectively.

5.2.3 Gate dielectric dependence

This measurement is conduct based on the OFET device with PMMA as gate dielectric and device with SiO2 as gate dialectic. Both devices have TC/BG configuration and 25μm channel length.

Figure 5.8 shows the output characteristics based on the sample with SiO2 as dielectrics. It shows p-channel transistor and clear linear and saturation regime. However, the trap issue is also obvious, which is as expected. At the interface between silicon dioxide and semiconductor electrons is trapped by hydroxyl groups and thereby prevent their transport through the transistor.

The mobility also can be obtained in the earlier mentioned way.

$$\mu_{lin}\Big|_{SiO2,V_{ds}=-10V} = 9\cdot 10^{-9}\cdot\frac{25}{26000\cdot 1.15\cdot 10^{-8}\cdot 10} = 7.5\times 10^{-5}(cm^2/V\cdot s) \quad \text{(Equation 5.6)}$$

where channel length is 25μm, channel width is 2.6cm, the slope of source drain current to gate voltage obtained in linearity fitted from Vg = -50V in transfer characteristics is $9*10^{-9}$A/V. Ci is the insulator capacitance per unit area between gate and semiconductor, which is calculated as follows:

$$C_i = \frac{k\varepsilon_0}{d_{SiO2}} = \frac{3.9\cdot 8.85\cdot 10^{-12}F/m}{300nm} = 1.15\times 10^{-8}\,F/cm^2 \quad \text{(Equation 5.7)}$$

From the calculated mobility, Silicon dioxide also shows inferior performance than PMMA gate material, indicating the limitation of SiO2 used in OFET, for instance, trap issues.

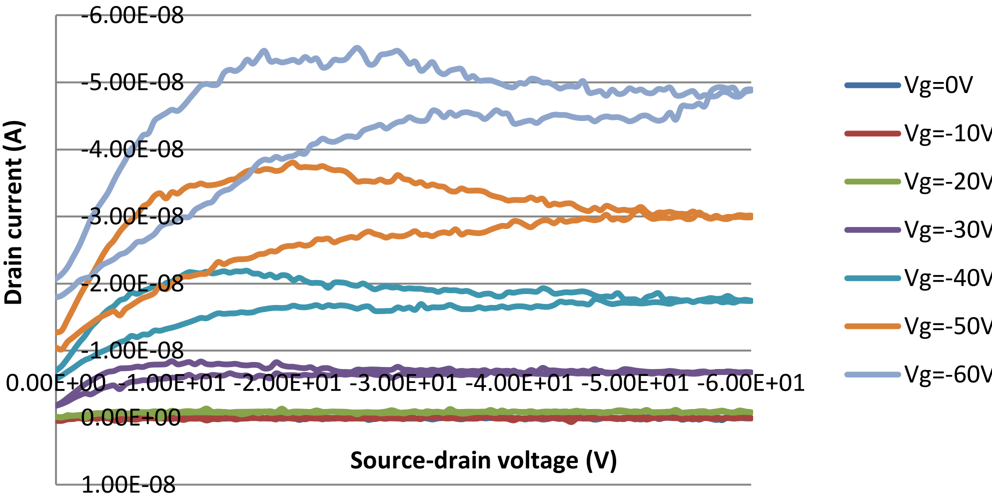


Figure 5.8 Output characteristic sweeping Vds from 0V to -60V based on the sample with SiO2 as gate dielectric

5.2.4 Electrode material dependence

Both Gold and aluminum metal material are used to works as source and drain electrode of OFETs. Since the HOMO and LOMO energy level of PPTTPP semiconductor are 5.3eV and 2.8eV respectively, the OFET with gold (5.1eV) electrodes is expected to be p-channel transistor, while OFET with aluminum (4.28 eV) is expected to be ambipolar transistor. However, the work function of aluminum is still close to the HOMO level, which may lead to an undesired ambipolar behavior.

Figure 5.9 and figure 5.10 show the transfer characteristics of aluminum OFET in positive and negative direction. When observing one of the curves with a constant Vds, it shows the current states to flow at high enough gate voltage in the negative direction. It indicates that a p-channel transistor, where hole transport in the channel. However, the current does not increase systematically with Vds, which deviates from the expectation. So here I only can conclude a p-channel behavior with poor electrical contact. The reason can be explained with the high contact barrier between the PPTTPP and aluminum, which leads to the energy level of aluminum does not matching well with PPTTPP. And the contact barrier perhaps does not keep constant during the measurement. In short, both gold and aluminum electrodes exhibit p-channel transistor while aluminum appears worse contact.

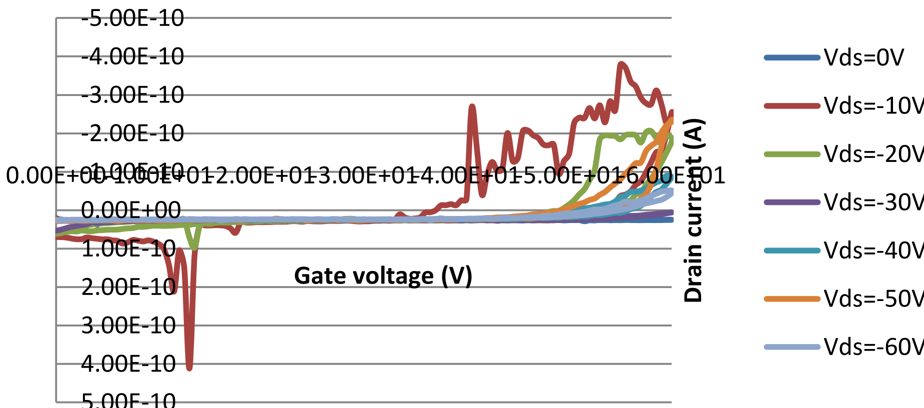


Figure 5.9. Transfer characteristic sweeping Vg from 0V to -60V based on the sample with Al as source and drain electrode

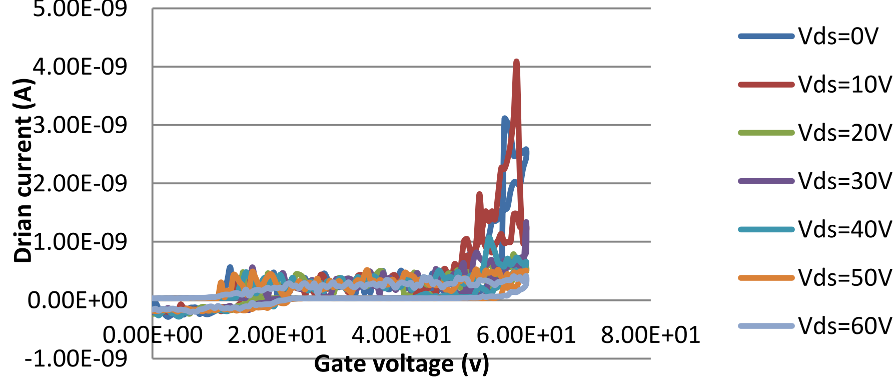


Figure 5.10. Transfer characteristic sweeping Vg from 0V to 60V based on the sample with Al as gate dielectric

CHAPTER 6 CONCLUSION AND OUTLOOK

In this project, an OLET is developed as the structure as follows: PPTTPP thin film acting as organic semiconductor is connect to gold (Au) source and drain electrodes, which is positioned on top of PMMA layer on Au bottom layer. Poly(methyl methacrylate) (PMMA) is the optimized gate dielectric, which shows superior performance than SiO2. Aluminum (Al) also be investigated as source and drain electrode.

The configuration is classified by the relative positions of three electrodes (source, drain and gate) dielectric and organic semiconductor, creating BC/BG, TC/BG and BC/TG three configurations. And the configuration also affects the device performance and become an investigating factor in this project.

Another factor discussed in this project is the channel length, which is obtained by the design the stencil with different dimensions. Hence achieving the source and drain small pairs with 10 μm and 25 μm via deposition through the stencil fabricated as design.

With the device differing with configuration and channel length, electrical and optical measurement is conducted. In principle, by applying a voltage larger than threshold voltage to the gate, the conductance of the PPTTPP organic semiconductor can be modulated and under certain conditions, holes and electrons can meet to recombine and emit light.

The result of electrical measurement indicates a completely p-channel transistor, which is the polarity of major charge carriers in the transporting channel. Three types of OFET is classified as p-channel, n-channel and ambipolar devices, indicating holes, electrons, both charge carries respectively taking in charge of channel. This totally p-channel OFET is the outcome decided by active organic layer, dielectrics, electrode and even the environment. There is an injection barrier for the charge carrier to transport into organic semiconductors by driving voltages, whereas the LOMO and HOMO level of PPTTPP is around 2.8eV and 5.3eV respectively and the work function of the metal used in this project is 5.1eV (Au) and 4.28 eV (Al). It appears holes working as the majority charge carriers injected to HOMO level, which attribute to both gold and aluminum S/D device with p-channel behavior. Moreover, the optimized dielectric layer shows its benefits in the characterization of OFET device. PMMA contains no hydroxyl group, improve the device performance via reduced charge trapping and thereby result in higher energy efficiency compared to the conventional silicon dioxide (SiO2) layer.

Based on the I-V curve measured, holes mobility and threshold voltage can be obtained. The calculated holes mobility depends on channel length and configuration. And the top contact configuration, longer channel length, PMMA gate dielectric and gold electrodes gives the best performance the OFET devices. The result shows the mobility up to $9.69*10^{-3}cm^2vV^{-1}s^{-1}$, threshold voltage down to -13.3 V, low leakage current on the order of 10^{-9}A.

Based on the results, there are more experiments can be conducted in future,

- Investigating PPTTPP nanofiber as organic semiconductors. Compared with thin film, nanofibers show a more ordering PPTTPP molecule, thus may creating different morphology between active organic layer and dielectrics, different contact resistance between metal electrode and organic layer and thereby different device performance. Moreover, the charge transport may follow a better path in hope mode contributed to higher mobility

- N-channel and ambipolar OFET are two interesting types can be fabricated. It requires low work function metal to match the HOMO and LOMO organic semiconductor of because many organic semiconductor HOMO level ranges from 4.8ev to 5.3ev and LOMO level is around 2-3ev. One possibility is using another electrode material or organic semiconductor which the energy level can be matched. Besides, electrons trap-issue is also a potential problem.

- Optical characteristics can be look into the failure reason. In this project among TC/BG and BC/BG configuration OFET devices with different channel length fail to observe light emission from AC gated, which means organic light-emitting transistor (OLET) fail to realization. One possible reason can be the different life time between SiO2 and PMMA, A high operating frequency or thinner thickness PMMA can be future work to investigate.

- As discussed in section 3.2.2, PS and PI are reported with superior performance in OFET devices. Investigating these two materials as gate dielectric can also be a possible future work.

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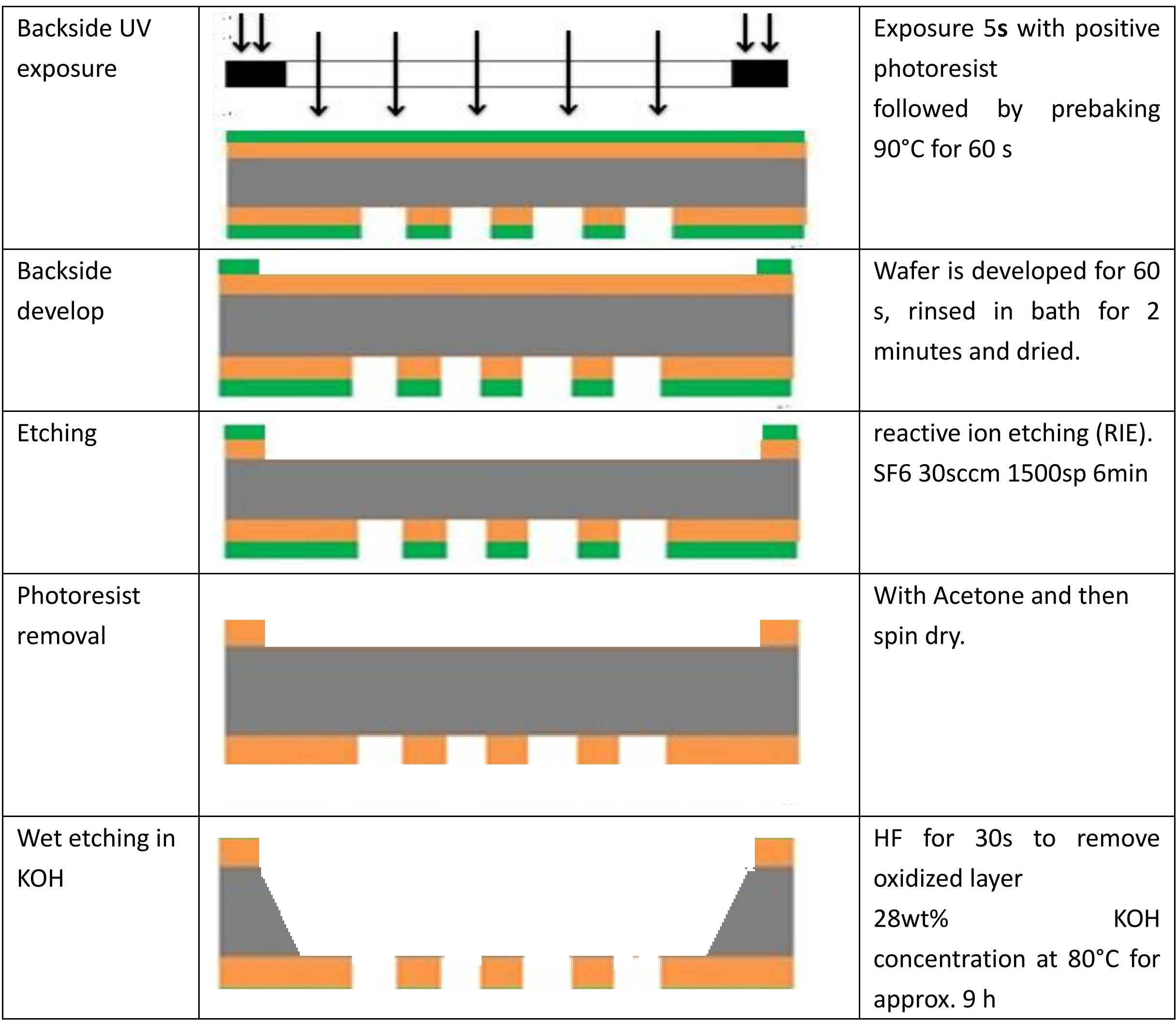
APPENDIX A: WAFER USE LIST

wafer	Diameter (μm)	Thickness (μm)	Dopant	Deposition	Use in this project
N1	100	525	P		Investigating break-down voltage
N5	100	400	P		OFET device
N7	100	400	P	100nm SiO_2	OFET device
P3	100	525	B	300nm low-stress silicon nitride	Stencil

APPENDIX B: FABRICATION RECIPE OF STENCIL

Process	Cross-section view	Remarks
Wafer prepared		300nm SIN on Si wafer
Photoresist application		**HDMS** EBS11 spin coater, resist: AZ5214E,resist thickness=1.5 μm: 1.Automatic resist dispense; 2. Spin at 500 rpm for 5s(acc. 5000 rps^2); 3. Spin at 4000 rpm for 30s(acc. 10000 rps^2)
UV exposure		Exposure 4 .3S with positive photoresist followed by prebaking 90°C for 60 s
Develop		Developer: AZ 351B (mix with DI water, ratio 1:4), 60 s, agitation, then Rinse in water (fine rinse bath) for 2 min, spin dry
Etching		reactive ion etching (RIE) SF6 30 sccm 1500sp 1min45s
Apply photoresist on backside		• Remove photoresist in acetone, rinse in DI water • HMDS • Spin photoresist on front side (4000 RPM) + prebake • Spin photoresist on back side (3000 RPM) + prebake



Backside UV exposure		Exposure 5**s** with positive photoresist followed by prebaking 90°C for 60 s
Backside develop		Wafer is developed for 60 s, rinsed in bath for 2 minutes and dried.
Etching		reactive ion etching (RIE). SF6 30sccm 1500sp 6min
Photoresist removal		With Acetone and then spin dry.
Wet etching in KOH		HF for 30s to remove oxidized layer 28wt% KOH concentration at 80°C for approx. 9 h

APPENDIX C: FABRICATION RECIPE OF OFETS

OFET Based on BC/BG configuration

Process	Cross-section view	Front view	Remarks
Wafer prepared			100nm Diameter, 400μm thickness, <100> orientation, P-doped Si wafer
Spin photoresist			HMDS EBS11 spin coater, resist: AZ 5214E,resist thickness=1.5 μm
Dicing wafer			6μm*10μm chip
Remove photoresist			
Deposition Ti and Au			3nm Ti and 30nm gold
Spin PMMA			5s 500rmp and 45s 2000rmp with A7 to achieve 400nm thickness
metal deposition with shadow mask			e-beam PVD with 30nm (gold or aluminum)
metal deposition with stencil			e-beam PVD with 30nm (gold or aluminum)
PPTTPP deposition			

OFET Based on TC/BG configuration

Deposition Ti and Au			3nm Ti and 30nm gold
Spin PMMA			5s 500rmp and 45s 2000rmp with A7 to achieve 400nm thickness
PPTTPP thin film deposition			30nm deposition
big electrode			30nm gold or aluminum
Small electrode			30nm gold or aluminum

APPENDIX D: EXPERIMENT EQUIPMENTS AND DETAILS

Cleanroom processing equipments:

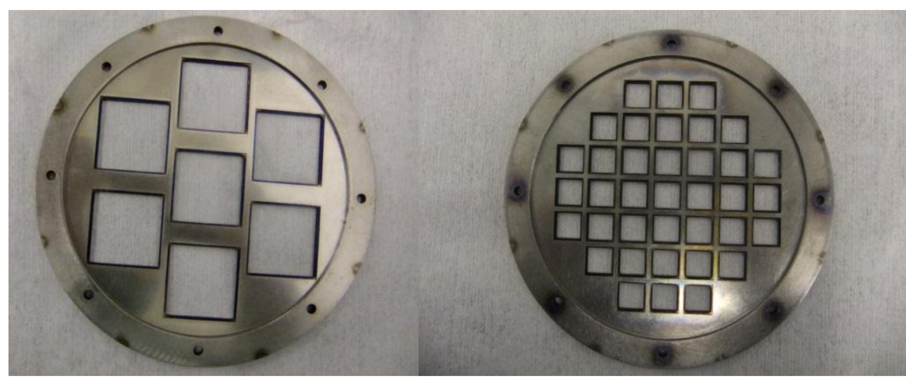
1. Cryofox Explorer 600

The Cryofox Explorer 600 applies deposition of metal and dielectrics via magnetron sputtering and electron beam evaporation. In e-beam deposition, normally gold (Au), sliver (Ag), aluminum (Al) and titanium (Ti) are placed in e-beam pocket 1 to 4 respectively. It is also able to conduct DC sputtering and RF sputtering deposition. There are different sample holders available for the instrument, including 25*25μm, 10*10μm holes sample holder and so on.

In this project, Cryofox is used in following processes: deposition Ti and Au bottom electrode layer of OFET device via holder shown in figure, deposition source and drain electrode of OFET device via holder shown in figure, deposition source and drain small pairs of OFET device via stencil, deposition Ti and Au bottom electrode layer of substrate used in investigating breakdown voltage.

Figure show this instrument, which consists of two chambers, the upper one is the transfer chamber to place substrate, the lower one is the main chamber to place target. The procedure can be simplified as the following step: setting deposition parameters, taking Ti and Au bilayer deposition as an example, the detail fabricating parameter is shown in table D.1; loading sample in after ventilating the transfer chamber, via suitable holder chosen by the size and shape of the sample; starting deposition process by pressing coating process and start/stop button; pressing start layer button when the chamber pressure reaches the setting value and switch sweeping program to corresponding pocket number; unload sample when the deposition ready and the transfer chamber will automatically vent.

Figure D.1 image for Cryofox 600 Explorer deposition machine



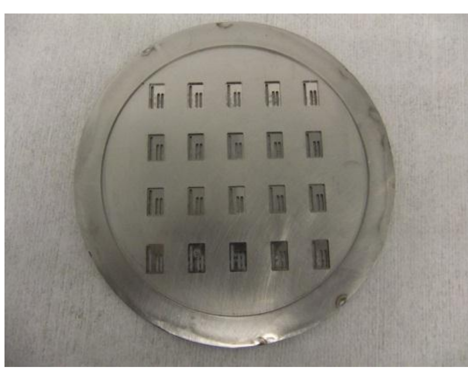


Figure D.2 shadow mask with 25*25μm (top left); 10*10μm (top right); rough electrodes aperture used in OFET (bottom)

	Layer1	Layer2
Materials	Titanium	Gold
Thickness (nm)	5nm	30nm
Base pressure(mbar)	$3x10^{-5}$	$3x10^{-5}$
Rate (Å/s)	1.0	1.0
Pocket No.	4	1
Tooling factor	87	71

Table D.1. Deposition parameters for Ti and Au layer based on Cryofox. Parameter indication: Pocket No.: material selecting factor (No.4 refers to Titanium, No.1 refers to gold). Tooling factor: correcting factor for uniformity (Ti: 87~84 and Au: 71~70)

2. Digital inspection microscope (Nikon LV100D)

This is a digital optical microscope uses visible light and a system of lenses to realize magnify images of the sample. This instrument consist of five different magnitudes, which are 5times, 10times, 20times 50 times, 100times. In this project, it is used for the following procedure: checking particles in cleaning procedure, alignment with substrate and stencil, checking dimension of OFET and stencil substrate, taking images.

Figure D.3 image for optical microscope

3. Optical lithography setup

Optical lithography is a process used for transferring a desired pattern to a photoresist on the substrate through a mask in UV light illumination process, then chemical treatment and etching process producing pattern to substrate. This lithography setup consists of the following instruments: HMDS machine, spin coater, hot plate, mask aligner, developer bath, ICP RIE machine, resist strip bath. In this project, this setup is used in stencil fabricating process.

(1) HMDS treatment oven

This instrument is used for deposition a monolayer of Hexamethyldisilane (HMDS) onto the prepared wafer. The system need to heat up to 120℃ and the whole process takes around 30 min.

Figure D.4 image for HMDS machine

(2) Spin coater (RRT Lanz EBS 11)

In this project, AZ5214E resist is used to spin onto the wafer by EBS11 spin coater. With automatic resist dispensed, the spin speed of 500 rpm for 5s (acc. 5000 rps2) and 4000 rpm

for 30s (acc. 10000 rps2) is applied to the resist to achieves1.5 μm thickness uniform layer. It should be noted that the wafer need to put in the center of the plate and a test wafer need to be used before the target wafer. It can avoid ununiformed layer and possible spot and bubbles, which result from small amount of photoresist left in the bottle or a new bottle of photoresist.

(3) Hot plates

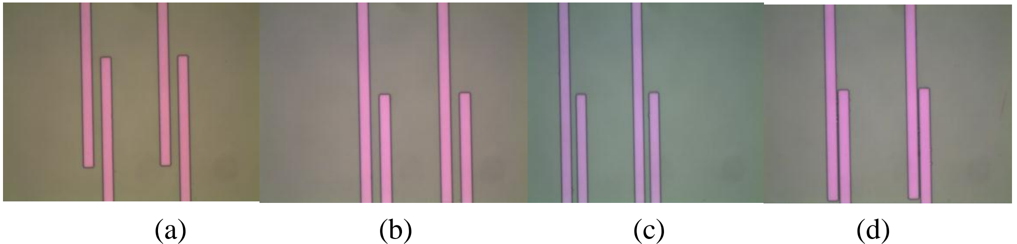
The hot plates (H. Gestigkeit PZ28-2SR) are used for substrate baking. In the lithography process, the substrate is baked at 90 ℃ for 60 s after spin coating in order to strengthen the bonding between HMDS and the wafer and remove the remaining solvent in the photoresist. Noted that the interval between the end of spin coating and the beginning of baking should be minimized, for the purpose that avoid aggregation of the solution and forming droplets thereby degrading the uniformity of PMMA layer thickness.

Figure D.5 image for Cryofox 600 Explorer deposition machine

(4) Mask aligner

The mask aligner uses UV light to produce pattern from mask to the wafer. This instrument is equipped with a 350 W Hg lamp and features both front- and backside alignment in proximity and contact printing. And it is recommended to check the status of mask before exposure under optical microscope.

In the stencil fabricating process, the front electrode pair side exposure time is 4.3second and back window side exposure time is 5 second. And the exposure time of front side is decided by comparing the performance among 4.0s, 4.3s, 4.6s and 4.9s.



(a) (b) (c) (d)

Figure D.6 image for stencil with different exposure time (a) 4.0s; (b) 4.3s; (c) 4.6s; (d) 4.9s

Figure D.7 image for mask aligner

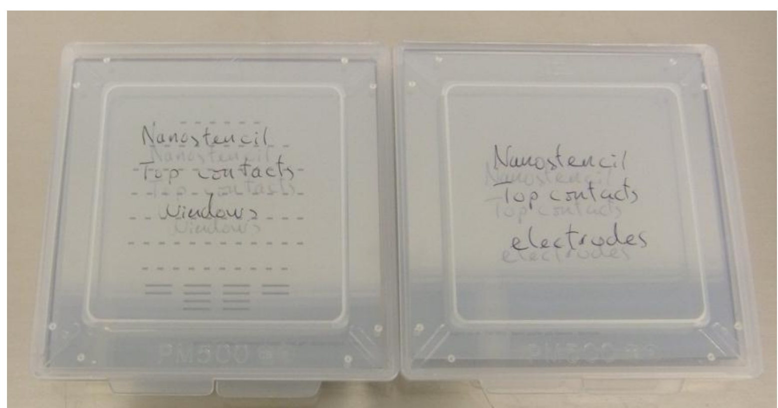


Figure D.8. Image for stencil mask, one is window mask (left), the other is electrode mask (right)

(5) ICP RIE system

Inductively Coupled Plasma Reactive-ion etching (ICP RIE) uses reactive plasma to bombard the substrate surface. A typical system consists of two electrodes and an electric field between them. Wafer gets into the system by placing in the wafer platter, which is electrically isolated from the chamber. The ions between the electrodes are generated from the gas pumped into the chamber. Here, SF6 works as source gases. Sulfur hexafluoride (SF6) produce Fluorine toward the surface of the samples.

In the stencil fabrication process, etching time is one of crucial parameter to create the stencils. Etching time has been investigated for different value to obtain desired stencil. Figure shows a low etching time. It is obvious that particle stays in the aperture area, thus means that the holes are not though. Figure show a high etching time leading to a curve shape stencil.

Figure D.9 image for ICP RIE machine

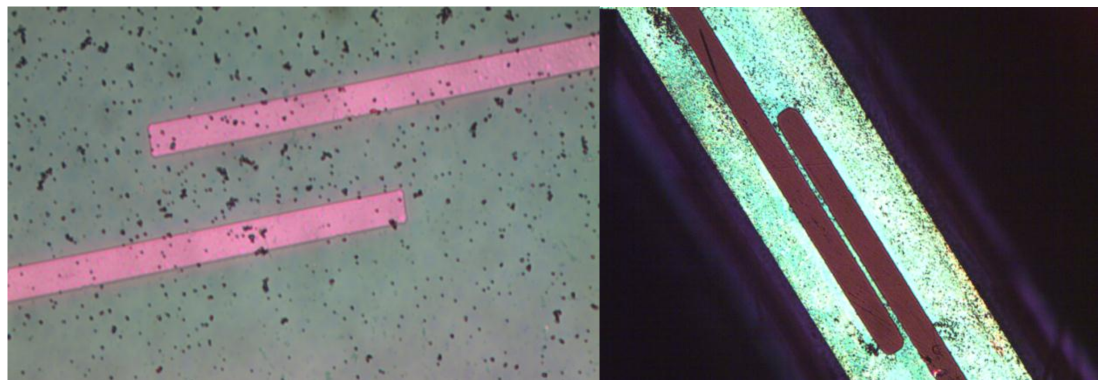


Figure D.10. Optical image for the failure stencils. Left is the stencil with not through aperture and right is the distortion stencil

4. Spin Coater (RRT Lanz EBS 11) and Hot plate (H. Gestigkeit PZ28-2SR)

In this project, spin coater and hot plate are also used for deposition PMMA layer in OFET device working as dielectrics and breakdown voltage measurement. In the breakdown voltage measurement, different thicknesses have been investigated ranging from 100nm to 800nm. And in fabricating OFET device is used as 400nm thickness PMMA.

The coating procedure of PMMA is a little different from photoresist spin coating. First, blowing the pipe is used to extract the PMMA from the bottle, in case of some particle left in the pipe thereby bringing to the substrate. A pipe can only put into the bottle once in order to avoid contamination to the original PMMA. Hence, it is recommended for pipe to have enough PMMA at one extraction. Then the amount of dropping PMMA should also be cautious. Too much amount may flow into the vacuum system causing the vacuum blocked. Accordingly, acetone should be used to rinse the spin holder in the first place. Besides, the thickness PMMA is not only decided by the spin speed and rotation but also the type of PMMA. Here three type of PMMA have been used in order to obtain different thickness. Standard PMMA products produce with 495,000 or 950,000 molecular weight (MW), and the A2, A4, A7 is all based on 950,000 MW. After spin coating, the substrate is prebake at 200℃ for 60s to remove the remaining solvent from PMMA layer. The interval also should be minimized.

Achieved PMMA thickness	5s	45s	PMMA type
100nm	500rpm		A2
150nm	500rpm	7000rpm	A4
200nm	500rpm	4000rpm	A4
300nm	500rmp	2000rmp	A4
400nm	500rmp	2000rmp	A7

Table D.2. Spinning parameters for different PMMA thickness

5. Developer bath

The developing process is taken place in developer bath and the developer is mixed AZ 351B with DI water in the ratio of 1:4. The quality of developer is sensitive to the temperature, hence temperature remains 22℃ during the developing process. In the stencil fabricating process, the wafer develops for 60s and rinse in wafer for 2 min. dryness is conducted via spin dryer.

Surface Science laboratory (Blok A, 3rd floor)

1. Probe station

Probe station consists of a Stanford Research SR570 current pre-amplifier, a 16-bit National Instruments DAQ card, Falco system WMA-02 and WMA-280 DC voltage amplifier and three probers, which is illustrated in Fig. the sample is connected by source, drain and gate electrode. The source get the input signal from SR70 current pre-amplifier, which is grounded, the drain and gate are connected with the output of DC voltage amplifier with 20 times signal multiplier. Then the signal is gathered by DAQ device adaptor, and finally sent to DAQ card, which can only provide maximum 10 volt.

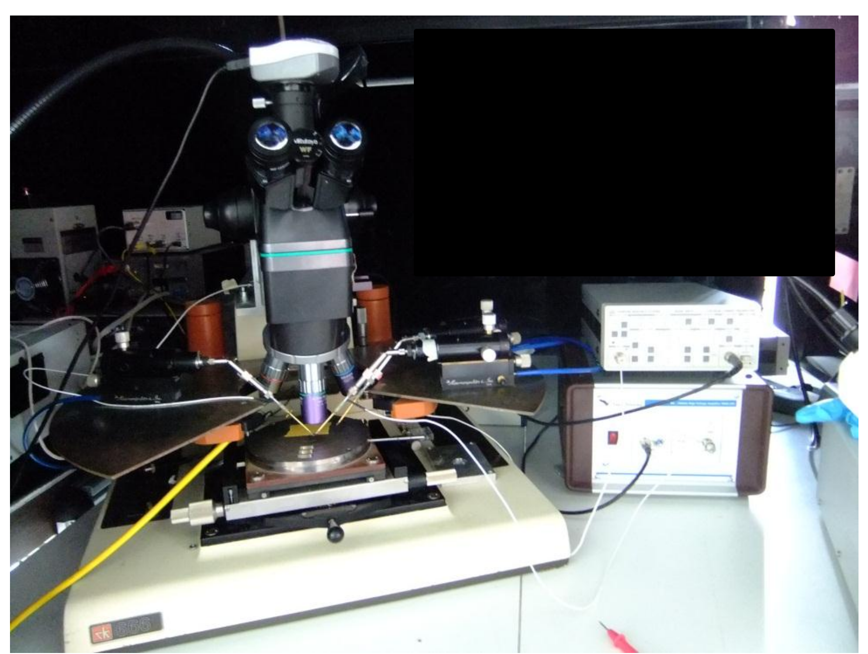


Figure D.11 image for probe station

2. Edwards R500 deposition machine

Similar with Cryofox Explorer 600, Edwards R500 is used for realizing thin layer deposition. Both electron beam evaporator and thermal evaporation can be conducted in this machine. This instrument allows applying up to 4 different materials

In this project, Edwards is used in the step of deposition sliver (Ag) electrode layer of substrate used in investigating breakdown voltage via the shadow mask shown in figure and the detail fabricating parameter is shown in table D.3.

Figure D.12 image for Edwards R500 deposition machine

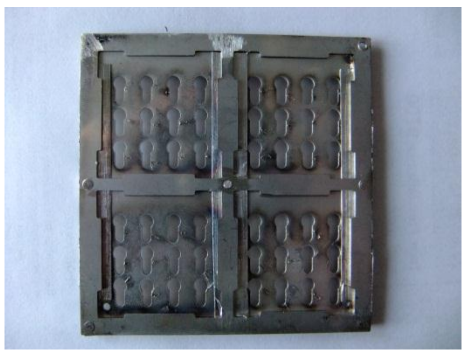


Figure D.13 image for shadow mask using in the breakdown voltage experiment sample to create electrode

Material	Silver (Ag)
Thickness	80nm
Current	20mA
Pressure(mbar)	$2.5x10^{-5}$
Rate	0.2nm/s

Table D.3. Deposition parameters for Ag layer based on Edwards deposition machine.

3. PPTTPP chamber

The chamber is used for deposition PPTTPP thin film or nanofibers. The initial conditions of the chamber are pumped down condition, rough pump open, turbo pump closed. The depositon parameter used in this project is shown in table D.4.

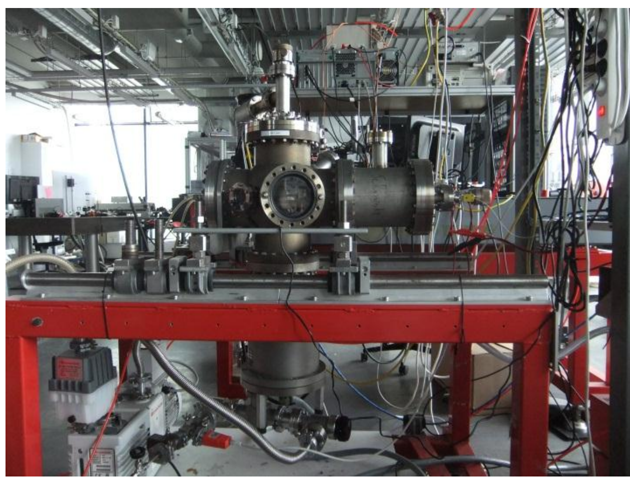


Figure D.15 image of PPTTPP chamber

	PPTTPP thin film
Base pressure(mbar)	10^{-8}
Oven supply	2.2A
Oven temperature(℃)	390(with prebake 250)
Deposition rate(Å/S)	0.25-0.31
Thickness(nm)	30

Table D.4. Parameters of deposition of PPTTPP thin film

APPENDIX E: OPTICAL EXPERIMENT SET UP

Based on the operating principle, the optical experiment set up is illustrated in figure E.1 The source and drain is applied with the DC voltage, where the source is connected with the negative and the drain is connected with the positive. AC sine voltage is connected with gate voltage. The experimental sample is under vacuum circumstance facing the optical lens. After setting the parameters of camera exposure time, frequency of AC gate voltage, light emission measurement can be conducted.

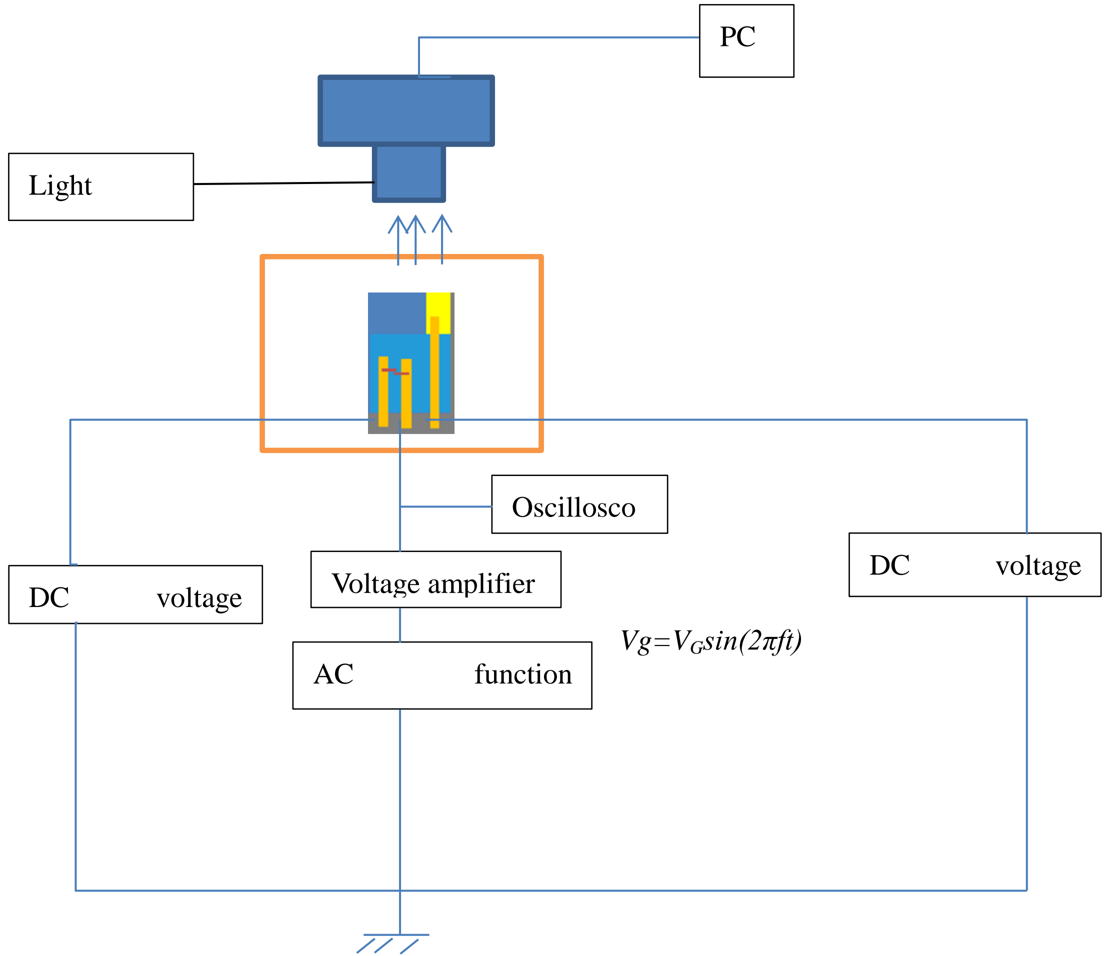


Figure E.1 Schematic diagram of optical measurement setup