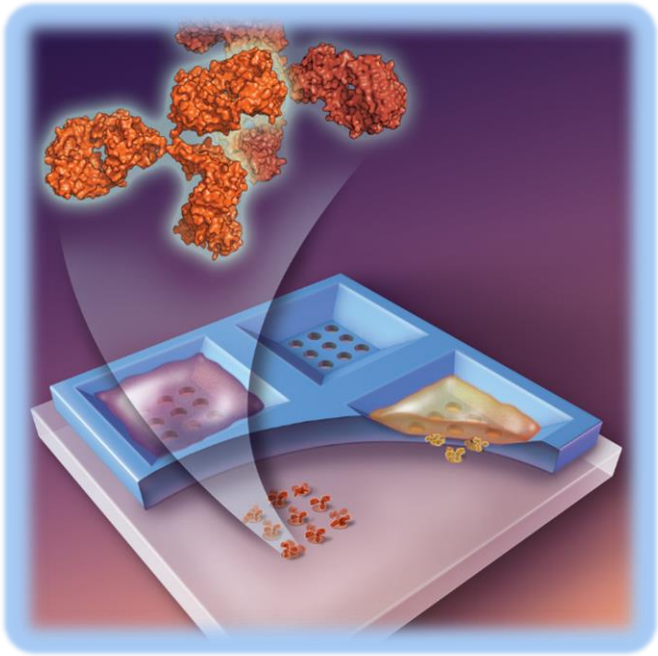
Bachelor Project

Nano-stenciling for fabrication of metal nanoparticles



External sensor: **Maria Dimaki**

Supervisors: **Jakob Kjelstrup-Hansen, Ole Albrektsen**

Submission date: **31.05.2013**

Student: **Ilias Esmati**

In corporation with MCI SDU Sønderborg/ Odense and Nano-SYD

Acknowledgements

Clean room facilities have been invaluable resource that has been critical in conducting my experiments. During working in the clean room for this project, I had the opportunity to meet and learn from professors and students and I would like to thank them all who helped me for utilizing the equipments.

Firstly I have to thank my supervisors Jakob Kjelstrup-Hansen and Ole Albrektsen for their kind support. In addition I would like to mention Jacek Fiutowski and Kasper Thilsing Hansen for their support in the clean room

Finally and most importantly I would like to thank my friends, family and of course my wife, who they have given me more loving support than I could ever ask for.

Author:

Ilias Esmati

_____

Exam nr: 198634

Table of Contents

List of figures

List of tables

1. Abstract

Nano scale fabrication with controlled dimensions on the Nano meter scale precisely positioned on a suitable surface is one of the ultimate tasks for stencil lithography, where it is a promising candidate for Nano scale application with high throughput, low cost and reliable.

In this project Nano scale rectangular shape with dimension of 210nmx180nm in a matrix form of 50x50 in a working area of $18\mu m\ X\ 18\mu m$ is transferred into low stress Silicon Nitride membrane of approximately 300 μmX450 μm supported by 5mmX5mm silicon stencil holder.

Primarily this project should have addressed the investigation of multiple use of a Nano stencil mask with focus on its influence on Surface Plasmon Resonances (SPRs), but due to the formation of crack lines on the surface of low stress Silicon Nitride membrane after Reactive Ion Etching the focus of this project has been shifted to optimize the steps of stencil fabrication to prevent the formation of cracks. The Formation of crack lines after performing RIE to etch the predefined pattern into the membrane precludes further usage of the stencil. The crack lines make the thin silicon nitride membrane vulnerable, as even after first metal deposition through the stencil, the membrane breaks, hence a series of systematic hypnotically approach has been conducted to trace at which step does the crack lines occur at.

It has been investigated that the crack lines are essentially due to thermal stress on the surface of the membrane, where prebake time and temperature has been optimized to some extent.

Using the optimized recipe for Nano- stencil fabrication, due to limitation of time only one successful metal deposition has been carried out; where after the second deposition the membrane was broken due to the stress on the membrane surface. Moreover, a suggestion of future projects along with detailed setup has been addressed.

2. Introduction

This project is heavily based on experimental work that has been conducted in the clean room (SØNDERBORG), where more than 210 hours has been spent in the clean room both for self-learning the equipment utilization and data collection through experiments.

It was really important to have a flexible and yet clear plan, using the equipment, especially the SEM, where only 2 hours were allowed per/day. In this work, a systematic approach to the problem solving has been carried out, for example during optimization only one factor at a time has been tested and analyzed.

The project is divided into sections; first a foundation is laid for the reader to understand the background materials needed and then tests has been presented. In the optimization section, each factor has been carefully tested, first by claiming a hypothesis, followed by and setting a reasonable experimental setup. In the optimization part, the data is presented in a step by step changing the factors and the results and observations are discussed and interpreted in later section followed.

The project formulation is not totally addressed due to the problem formation of the cracks, on the silicon nitride membrane; hence an optimization on how to prevent the formation of the cracks on the membrane, was initiated in order to go further to address the project problem.

A systematic optimization on pre-bake time, temperature, metal deposition and Reactive Ion Etching lead to a reasonable recipe for stenciling, but the formation of the crack lines on the membrane surface has not been totally eliminated, therefore only one factor has been left un- tested; that being COLD DEVELOPMENT, for which, there was no equipment available.

Using the optimized recipe, which can be used to transform the pattern by metal deposition, only single time, due to stress and increase in weight on the membrane, the cracks can get large enough so the whole membrane breaks precluding further usage. Furthermore, in further sections of the project, it has been clearly stated how to continue, and which factors are potentially important and thus to be tested.

3. Problem statement/research question

3.1 Project formulation

The aim of this project is to develop a Nano stencil-based process for fabricating Plasmonic nanostructures which has specified surface Plasmon resonances (SPRs). Specifically, it will be investigated how the multiple use of a stencil mask will influence the SPRs of the resulting nanostructures. The final aim of the work is to demonstrate how this technique can be applied to produce substrates for surface-enhanced Raman spectroscopy, more specifically how a single Nano stencil mask can be used to fabricate a series of substrates carrying nanostructures having SPRs within a pre-specified wavelength range

3.2 Project delimitation

- Electron beam lithography
- Electron beam deposition
- Reactive Ion Etching, Wet etching techniques
- Linear reflection spectroscopy
- Nano –stenciling

Instruments used:

- Atomic force microscope (AFM)
- Scanning electron microscope (SEM)
- Cryofox 600 system equipped with E-beam evaporator and sputter sources
- Inductively coupled plasma ,Reactive ion etching (ICP RIE) system
- Optical microscope equipped with CCD camera, spectrometer, lamp source

4 Background

Metallic nanoparticles can support plasmonic resonances, in which an incoming light beam interacts with the free electrons in the metal, and thus concentrate the energy in the near-field around the particle. Such plasmonic effects can have a number of applications, for example, molecular sensors in which the field enhancement near the particle can cause an increased sensitivity, and in solar cells, where the incoming energy can be concentrated in the active layer and thus provide the basis for increased efficiency in energy conversion. The resonant frequency, where the incident light couples most effectively to a plasmon1-state depends on the material (*typically, gold*), and of the particle dimensions.

A Plasmon resonance frequency in the visible part of the spectrum typically requires particle size in the sub-micron (e.g., 0.1 micron) region. In order to achieve particles of this size it is therefore necessary to use a Nano- lithography technique, typically electron beam lithography "EBL" which can define the particles of the desired size. However, this technique has some potential disadvantages including the process being relatively time-consuming and can be performed only on certain types of substrates. An alternative technique is so-called “Nano-stenciling”, which is using a mechanical shadow mask consisting of a thin membrane with nanometer-scale perforations to realize metal particles by deposition of metal through the shadow mask. However, a potential issue with Nano-stenciling is that multiple depositions through the same shadow mask can result in clogging of the holes in the shadow mask leading to smaller deposited particles.

4.1 Electron beam lithography

Electron beam lithography (EBL) is a fundamental technique, used in nanofabrication. This technique enables to write down to sub 10nm dimensions and on the other hand it also enables to create high volume Nano scale patterns using optical lithography and Nano-imprint lithography through formation of templates and mask [1].

Transforming a desired pattern into a substrate requires a resist, i.e. PMMA or poly-methyl methacrylate which is a long chain polymer with 950kDa, is used as electron beam positive tone resist. When exposed to e-beam it undergoes a conversion from low to high solubility, where the polymer is broken to smaller fragments fig. [1b] the desired pattern can get shape on PMMA after development process fig. [1c] later it can be used to either etch through the substrate or metal is deposited on PMMA followed by a lift off, where PMMA is removed allowing the metal to sit on the substrate.

Electron beam lithography has an advantage where the electron beam can be reduced to 1nm and has a good flexibility where all patterns are under computer control. However the disadvantage of EBL is its cost and need for high vacuum and precision electron focusing magnets, and on the other hand it is a very time consuming process where only one pixel is exposed at a time meaning that it is not commercially viable except for a few application

Despite E-beam lithography provides a high resolution, it has an undesired factor which the adjacent region exposed to beam gets affected by scattering electrons in the resist and the substrate. This effect is called proximity effect. This proximity effect [2] is responsible for intended size variation Factors that limits the resolution of e-beam lithography is the electron optic aberration and scattering of electrons in the resist and substrate. As the electron enters the resist and substrate two things happens to electrons either they are forward scattered or backscattered.

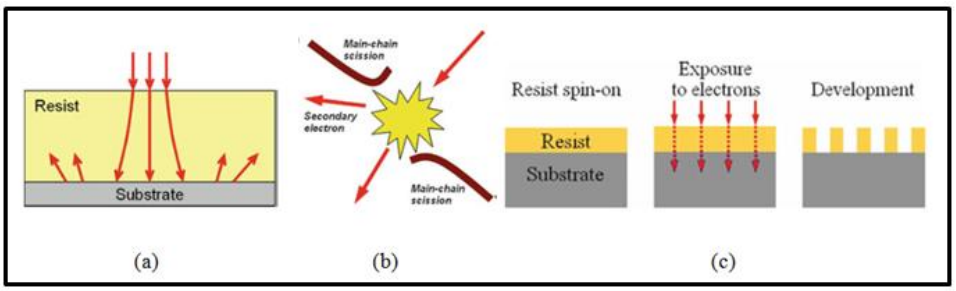


Figure 1 a) e-scattering (b) PMMA (c) development process

Forward scattering

The electron collides with the one of the electron from the resist/substrate, this causes electron change path hence transfer its energy to the atom. This extra energy allows the atom to be excited where the electron goes to a higher energy level, when this electron leaves the atom a secondary atom would be created . This excitation or ionization would be the result of this excitation, but due to inelastic scattering the angle is quick small.

Backward scattering

This is due to elastic interaction of the electron with the nucleus, this causes the electron to change its path but retain most of its energy. Unlike the forward scattering the angle is much larger, hence there is a high chance that the electrons bounce back through the resist and cause an additional exposure with a significant distance from the incident beam. The proximity is caused because of this phenomenon of backscattering.

Because both cases occur when the e-beam lithography is performed hence it results a proximity effect which widens the exposure region. What is important when dealing with back scattering phenomenon is that the electron that are back scattered are strongly related to the substrates material, where a substrate with high atomic number results a larger backscattering compare to the substrate having a lower atomic number. The transfer energy when head on collision occurs with the nucleus.

$$E = \frac{E_0\left(1.02 + \frac{E_0}{10^6}\right)}{465.7A}$$

E_0: *incident energy*

A: *number of atom in the target*

From the following model it can be summed up as; (a) small scattering angle after the collision of the incident electron with target electron (b) large scattering angle after collision of the incident electron with the nucleus.

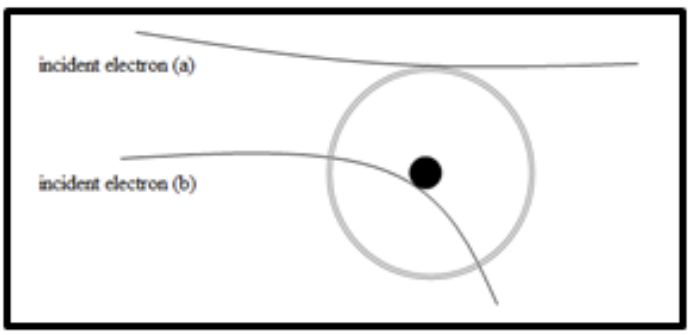


Figure 2. electron model

Performing electron beam lithography, a Scanning Electron Microscope is required, below is a brief description of SEM is described.

SEM has been around for more than 50 years, using SEM beat the diffraction limit of light. Any wavelength less than the wavelength of light would not be able to observe with microscope. An electron poses much shorter wavelength, the images that are much smaller than the diffraction limit of light can be seen by SEM.

The main parts are: The column, it is a cylindrical column, the chamber, the table, where the system is mounted on User console, to performed user manipulation.

At the top of the column there is a source of electron, called electron gun which is a tungsten filament and a strong E-field is used to draw all the current from that filament that is the beam used on the sample.

Below the electron gun there are two condenser lenses, scanning coils to move the beam, stigmators for rounding the beam and a probe lens at the bottom. As the beam exits the probe lens the sample absorbs the energies from the electrons and re- emits to view the new image.

The pressure on the chamber is in the order o -5mbr. The turbo pumps are used for vacuum purposes fig [3].

Performing EBL a high voltage approximately 30kV and 1uA is used, however lower voltages are good for biological samples whereas high voltage is good for good resolution.

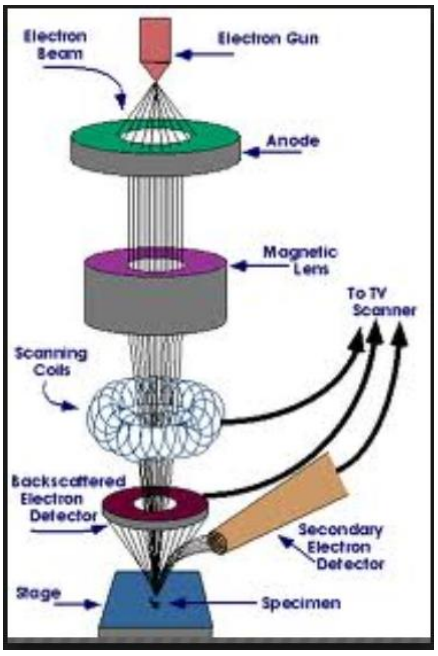


Figure 3. SEM

4.2 Nano stenciling

Stenciling is used in macro world for arts and crafts and decorative paintings; it is used to transfer a single pattern. A desired pattern is cut out on the stencil then pain or ink is applied through the aperture. This stencil shadows the applied agent around the pattern created. Nano stenciling lithography is exploiting this but in Nano scale. For instance too create gold Nano shape rectangles array, a rectangular Nano stencil is fabricated and gold is deposited through the apertures, when Nano stencil is removed (which can consist of a thin low stress Silicon Nitride membrane that acts as a mask to transfer the patterns from the membrane to the substrate during the evaporation) a gold Nano particle would remain on the substrate which is complementary to the Nano apertures used in the stencil. In contrast with Electron Beam Lithography that has been discussed earlier, its drawback is low throughput; each nanostructure has to be created on at a time which is both slow and costly [4]. Using EBL there is also another limitation at that is when EBL dependence on substrates conductivity. If a pattern is to be created on glass an additional layer of conductive layer should be applied such as (ITO), adding this layer may interfere with the optical responses of the fabricated nanostructures [5]. In the table below a comparison of pattering in different process (stenciling, Liftoff and etching) is shown [6].

Table 1, Stencil vs. liftoff and etching

Stencil	**Lift off**	**Etching**
		Metal deposition
	Resist coating	Resist coating
Alignment of stencil on substrate	Alignment and exposure through mas (EBL)	Alignment and exposure through mask EBL
	Resist	Resist development
Metal deposition	Metal deposition	Metal itching
	Resist lift off	Resist removal

The main advantage of stenciling is that it does not rely on photoresist processes, despite photolithography process is mainly used but it requires many steps, for example application of photo resists, exposure, development, evaporation of a thin film and lift off. Unlike photoresist method stenciling requires only on step procedure, where the desired pattern can be created.

The deposited structure can be used

- Directly
- Transferred into sub layer
- Combined by liftoff process

Nano stenciling has several of main advantages compare to other types of lithography's:

Table 2, Stencil Advangages

No resist, development or baking	Clean and soft technology
Non- contact	Pre-patterned
Re-usable	Rapid and low-cost patterning
Micro and Nano structuring (single step)	Wide range of size features
High flexibility of materials	Metals, oxides, piezoelectric

Nano stenciling has potential application [7] in:

- Nano electronics (high throughput with less than micro meter nanometer resolution)
- Nano biotechnology (patterning of in organic –organic interfaces)
- Nano scale material science (high flexibility of materials)
- Sensors

Modern stencils have evolved such that they enjoy use in many modes such as Static mode, multistep mode and dynamic mode. We are using static mode, where in this mode the structures with minimum blurring can be achieved, the sample is put inconstant with the stencil during the evaporation [8]

SL used ;SL method relies on direct deposition of material through a pre patterned mask, and the deposited material could be dielectric, metal deposition [9], Organic conductive molecules [10], Complex oxides [11], Self-assembled, monolayers SAMs [12], Polymer substrates [13] and CMOS devices [14]

Limitation

Despite the advantages Stencil Lithography (SL) has its own limitation where it has lower resolution compare to other techniques mentioned and the patterning area is also limited by the size and stability of the membranes [15], [16].

4.3 Reactive Ion Etching (RIE)

Reactive ion etching is a method used to transfer fine Nano size features from the mask to the wafer [17] or a substrate. In case of Nano stenciling the pattern is transferred into the low stress silicon nitride membrane by etching the membrane using reactive ion etching. First under low pressure plasma is generated by electromagnetic field [18] and a potential difference is created between the plasma and powered electrodes, where it allows the high energy Ions from the plasma attack the surface of the wafer, i.e. the silicon nitride membrane and reacts with it.

Plasma is basically initiated due to a strong RF electromagnetic field to the wafer platter. The field is typically around 13megahertz, applied at 1500watts. The oscillation electric field causes the gas molecules to ionize due to stripping them of electrons.

Electrons are accelerated up and down in each cycle of the field, when the electrons are stripped from the wafer platter, charge will build up due to DC isolation and this leads to a large positive voltage, typically a few hundred volts. Since the plasma possess high concentration of negative ions compare to the electrons a voltage difference builds up, hence negative ions tends to move towards the wafer and collides with the sample to be etched. Two things happen in this stage either the ions chemically reacts with the samples or knocking some of the material off by transferring their kinetic energy. The average energy of the Ions ε_{ion} can be defined by the potential difference in a collision sheath via

$$\varepsilon_{ion} = q * (V_p - V_{bias}).$$

Where q is the charge of an Ion, (V_p) is the plasma potential. Since (V_p) is very small compare to $V_{bias}$the ion energy is represented byV_{bias} A anisotropic profile can be produced in reactive ion etching due to the reactive ions that are mostly delivered vertically. Many types of RIE exist, the one in SDU Sønderborg **inductively coupled plasma** ICP RIE is utilized, and in this type of system plasma is generated using RF powered magnetic field Fig[4].

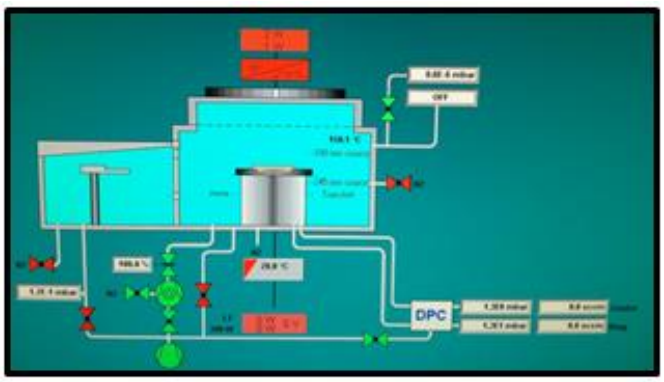


Figure 4. ICP RIE

This system is composed of two chambers a transfer and a main chamber. On transfer chamber the sample is mounted and the pressure is decreased to few hundred minibar and the wafer is transported to the main chamber, the wafer platter is electrically grounded. Gas enters the top of the main chamber through a small inlet and exits through the bottom. CF_6 gas is used and its amount is varied depending on the etching process.

4.4 Electron Beam Physical Vapor Deposition (EBPVD)

Electron Beam Deposition technique is used to deposit basically metal on a desired surface. In this project EBPVD is used to deposit Aluminum as a sacrificial layer to protect the PMMA in Reactive Ion Etching and to deposit Gold through the fabricated stencil. This technique involves bombardment of a target anode with electron beam, where the beam is generated using a high voltage by the tungsten filament under high vacuum Fig [5, left]. The beam is magnetically guided and collimated into a crucible containing material. The atoms from the target changes state from solid to gaseous due to the electron beam, where these atoms cover everything inside the chamber by making a thin layer of anode material precipitating as solid form. [19]

The advantage of using E-beam evaporation is its good for lift off and has highest purity. On the other hand it has disadvantage due its poor step coverage.

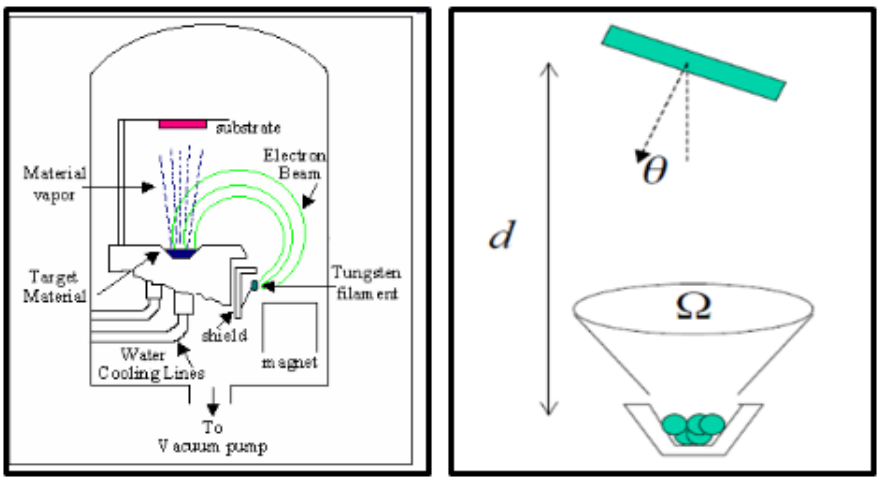


Figure 5 EBVPD

Deposition rate can be deduced using the following formula where r_{evp} is the evaporation rate, Ω: solid angle over which source emits, d: source to substrate distance, ρ: material density, θ: inclination of substrate away from direction to source.

$$devposition\ rate(\frac{thickness}{\text{sec}}) = \frac{r_{evap}}{\Omega d^2 \rho} cos\theta$$

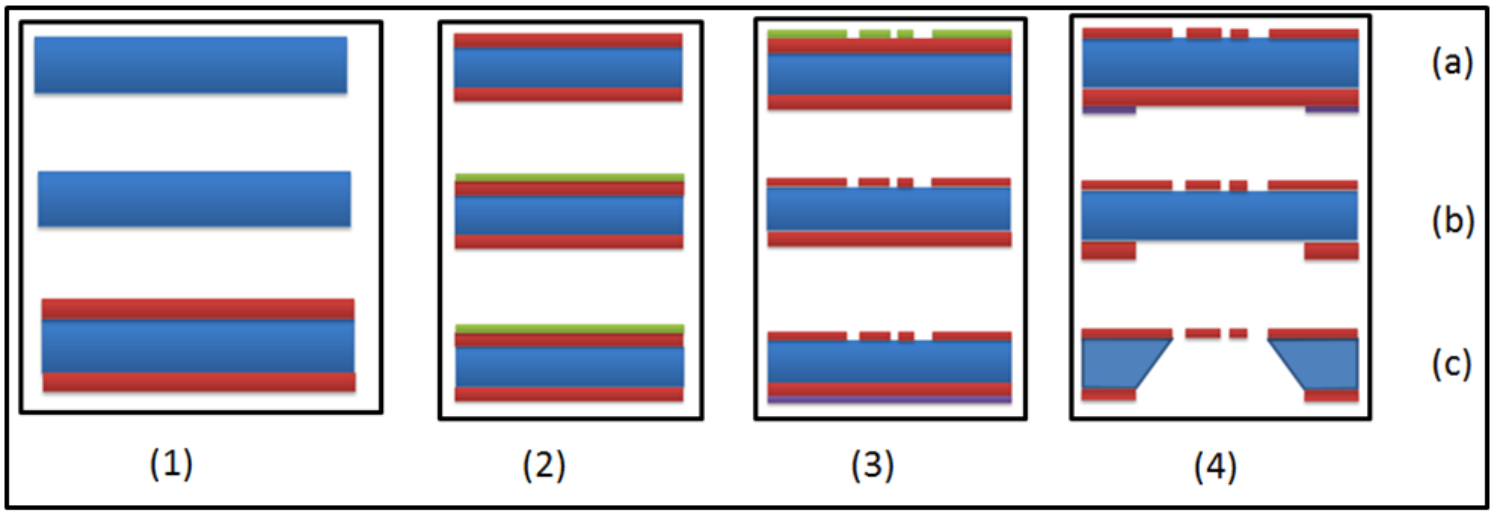
In this project during metal deposition of Aluminum layer as a mask, the wafer rotation is turned off; this makes sure that the wafer is level. This is important in case where Aluminum should be deposited at a specific angle.

5. Nano-stencil Recipe

Fabrication of Nano- stencil is performed in two steps, first fabrication of free standing membrane then the membrane is etched where the pre-defined pattern is transferred into low stress Silicon Nitride.

5.1 Fabrication of free standing membrane

The whole fabrication recipe of 100nm low stress Silicon Nitride as a free standing membrane is schematically demonstrated bellow.



1a: Silicon wafer

1b: material cleaning (DI water, Aceton, IPA and dry)

1c: Nitridation: coatting the wafer with 400nm thick LPCVD ,
SiN(low stress) layer (double sides)

2a: wafer cleaning with organic solvent

2b: *spi*nning 200nm + *p*hotoresist on front side , Methylmethacrylat (PMMA)

2c: 1hr bake in furnace 180C

3a: $mask\ 1,\ e-beam\ patterning\ of\ membrane\ structur,\ (micro\ structure)$

3b: $front\ side$: SiN dry etch with C_2F_6, (pattern transfered to SiN and SiO_2)

3c: back side: spining resist

4a: mask 2, back side lithography, defining membrane size: E − beam exposure

4b: $back\ side$: SiN dry etch with C_2F_6. Defining a 800 μm x 800 μm apertures on the bottom Using UV exposure, mask aligner and reactive ion etching RIE

4c: $ck\ side$: $selectivly\ etching\ Si\ by\ KOH\ anisotropic$, *(Stopping on top side* SiO_2) $2hr$ $(500nm\ thick\ SiN\ membrane\ releasing)$

Once the free standing membrane is fabricated, the wafer is cut into individual stencils, where the wafer is first by coating it with photo resist to protect against impurities during cutting process.

5.2 Fabrication of Stencil

To fabricate pre-defined Nano scale pattern 50x50 a top down fabrication method is used, where material is taken away to form those Nano scale objects.

In this recipe an optimized step by step of transforming of desired holes (design) to the Silicon Nitride is described.

Substrate preparation

- Remove the Photo resist using acetone for 5-10min and then with ISO Propanol followed with DI-water. Place the substrate at 100C hot plate for 1-2 min to make sure all solvents are evaporated

Remark: Ultrasonic agitation should not be used due to fragile membrane.

PMMA coating

A stencil holder is needed during the coating process, where the stencil is first mounted on the double tape and then place on the chuck that hold the silicon substrate 10x10 to ensure that the suspended membrane do not sag, otherwise the coated PMMA layer would not be uniformed and the silicon substrate can prevent the thin membrane to be pulled by vacuum under it. Use 950 PMMA A4

Program setting

Step 1:

- Time: 5sec, 1000rpm with a ramping of 1500

Step 2:

- Time : 45sec, 7000rpm and 10000ramping

Prebake

- Place the substrate on the hot plate for 30min at 150C

Electron Beam Lithography

- Perform EBL on the membrane (refer to Appendix for EBL setup, p.23)

Development

First develop the PMMA for 40s using (IPK) followed by 30 stopper then rinse the substrate with ISO propanol followed by DI-water

Place the substrate on 100C hot plate for 1-2 min to make sure all solvents are evaporated (it is a good idea to bring the sample for inspection using the optical microscope)

Remark: In order to achieve desired pattern, delay after EBL for development should be minimized.

Metal deposition

Deposit 30nm of Aluminum at a tilt angle of 70degrees with a deposition rate of 1 A/s using E-beam metal deposition.

Reactive Ion Etching

Etch the SiN membrane for 122s at 20C using 10watts of etching power in the presence of CF_6 300sccm under 2,2Pa.

- It is recommended to perform the RIE in four interval time; 30s,30s,30s and 32s to avoid the formation of crack lines on the surface of the SiN membrane

Lift off

- First remove the Aluminum layer using MF 322, by submerging the substrate for 30s
- Soak the substrate in acetone for 5-10min and rinse with ISO –Propanol followed by DI-Water.

6. Experiments

In this section a series of experiments are performed.

6.1.1 Exposure Dose

Dose factor value varies, depending wither EBL is performed on substrate or on a thin membrane. In these section two systematic experiments is conducted to determine a proper Dose factor for e-beam exposure.

An important factor during the EBL is the Exposure Dose, and it is dependent on resist, developer, temperature and energy. EBL is both performed on Silicon substrate and Silicon nitride membrane, due to their difference in thickness the exposure parameter differs significantly. Thickness of the material is important in this case due that the back scattering electrons depends on type and thickness of the material. The thicker the material more backscattering electron i.e. Silicon substrate, compare to 100nm Silicon Nitride membrane which is only 100nm. In case of thin membrane such as 100nm Silicon Nitride with e-beam resist most of the electron would pass through, whereas in Silicon substrate due to its large thickness most of the electrons are bounced back or backsctered, hence it is important to control the exposure parameter.

Dose factor tells us how much beam is exposed to the substrate on each point, to compare it with photolithography it is like changing the exposure time and it is the amount of electron per cnm^2 as function of position. Higher dose factor is needed for thin membrane such as 100nm Silicon Nitride compare to Silicon substrate due to back scattering, as mentioned before.

6.1.2 Dose test on substrate

When PMMA is exposed to e-beam it undergoes a conversion from low to high solubility, where the polymer is broken to smaller fragments, the longer the e-beam stays on a particular area the higher would be the exposure. And increasing the dose results a decrease in fragment size of the polymer where its solubility increases in developer, hence it is important to know what dose factor is the best for ones desired pattern. In order to find a suitable Dose factor a silicon substrate of 10mmX10mm was used to make the pattern with the dimension mentioned above, where this pattern was repeated with different Dose factor tests. Doses factor for the first trail was from 1.6 to 3.4 with interval of 0.4 and after the inspection with optical microscope it was clear that dose 1.8 gives a good result with dimensions; 213nmx183nm.

Setup

A 5mmX5mm Silicon substrate is coated with 950 PMMA A4, spun at 7000rpm for 45s prebaked for 90s at 200C and the pre-defined design is written on PMMA by EBL, where each design is tested with different Dose factor. The substrate is developed and 5nm of Ti is coated as adhesion layer at rate of 0.5A/s followed by 50nm Gold deposition at 1A/s rate. Lift off with acetone for 10min is carried out and each design with different dose factor has been studied with SEM in order to find the proper dose factor.

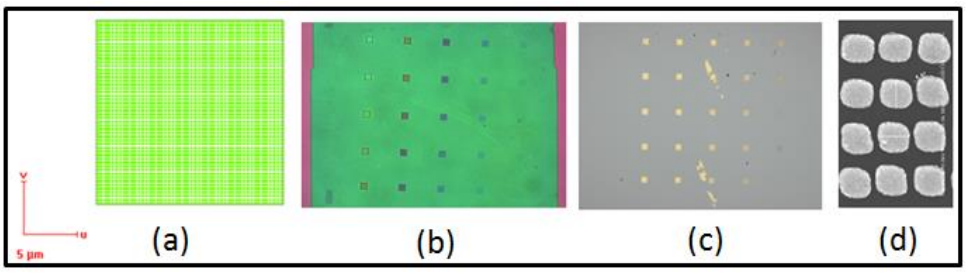


Figure 6.(a) design pattern 210nmX180nm in a matrix of 50x50 using ELPHY software tool. (b) each square is design pattern (a) with different dose factor. (c) Optical microscope image after metal deposition. (d) SEM image for single pattern with dose factor 1.8.

6.1.3 Dose test on Silicon Nitride membrane

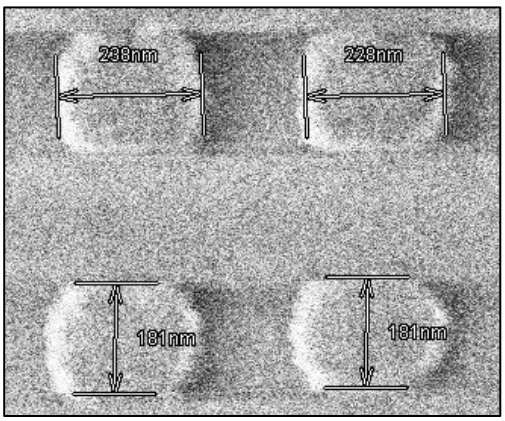


Figure 7.single dimension

Dose test is performed on suspended 100nm Silicon nitride using the same setup as for dose test on Silicon substrate. Determining a proper dose factor for silicon nitride two test is carried out, one with dose factors ranging from 3 to 10 and the desired output was found to be between 4 to 5 and on the second test a smaller interval has been taken from 4 to 5 with interval of 0.2 and inspection with SEM, dose 4.8 gives the best result 215nmX181nm

6.1.04 PMMA vs. Spinning Speed

PMMA is very applicable high resolution for electron beam lithography and is used as mask material due it is cheap and ease of removal [20] the following experiment is performed to determine the thickness of the PMMA at different speed. Where PMMA A4 is spun on Silicon substrate at different speed and the height before and after of the PMMA is measured using the Ellipsometer (refer to Appendix p.15).

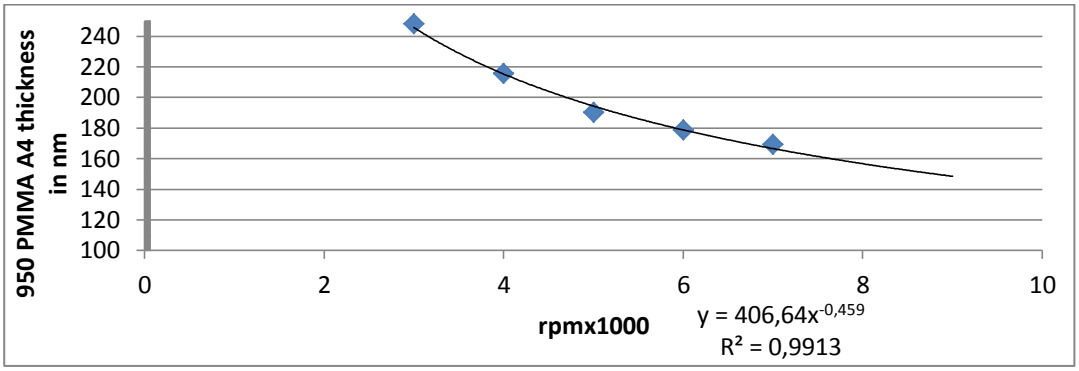


Figure 8.PMM vs. Spinning Speed

6.1.5 PMMA RIE Rate

The etching rate of PMMA using Reactive Ion Etching at 20C, 2.2Pa, and 80watts is tested at interval of 20s to 80s. 5mmX5mm silicon substrate is coated with 950 PMMA A4 and spun at 7000rpm for 45second (refer to appendix page). RIE is performed where only time is varied in order to determine the rate of etching. The height of PMMA is measured before and after RIE using Ellipsometer.

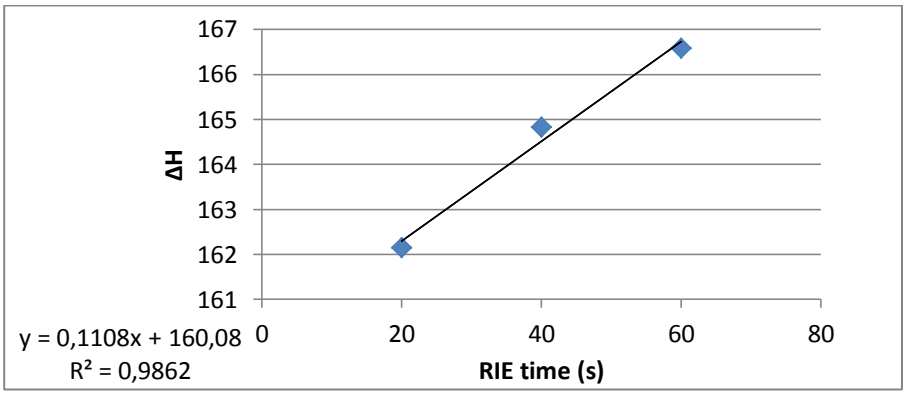


Figure 9.PMMA RIE rate

6.1.6 Silicon Nitride RIE Rate

Silicon nitride is chemically composed of silicon and nitrogen with formula Si_3N_4 [21] and in this section the etching rate of Silicon Nitride is measured.

The rate is determined by measuring the loss of Silicon Nitride layer in RIE, where a series of test is conducted at 10watts and 20C. For each setup all parameters such as temperature power and gas type are kept constant and only time is varied in interval of 20sec from 20 to 80s

Setup

1. The thickness of Silicon Nitride is measured using Elipsometer (refer to Appendix p.15)

Table 3, SiN vs time

Time (s)	T_B_RIE	error	T_A_RIE	error	Δ Thickness
20	55,8345	0,0584	43,8982	±0,0155	11,9363
40	90,537	±0,0465	61,556	0,0893	28,981
60	89,993	±0,0437	45,265	0,1085	44,728
80	91,173	±0,0476	29,626	0,1138	61,547

Table above represent the thickness of the SiN before and after reactive ion etching at 10Watts and

6.1.7 Silicon Nitride and PMMA Selectivity

In this section selectivity (SiN/PMMA) is determined to give a good understanding of how fast SiN is etch compare to PMMA

PMMA and RIE problem

One of the drawbacks of PMMA in RIE etching relative to silicon nitride membrane is that the PMMA is etched at about same rate as the silicon nitride. Hence a series of experiment is conducted to see how the power influences the etching rate of PMMA relative to silicon nitride membrane. Disadvantage of RIE is selectivity of etching which is not good. Because performing RIE on PMMA the PMMA would also vanish due to high etching rate in PMMA. This puts a limitation how deep we can etch. Maybe after 5min etching and all PMMA is gone. We cannot etch the holes very deep. If we have 200nm PMMA it means that we cannot etch 20μm perhapse 1 μm maximum or less.

It is therefore important to know how fast is the etching rate in PMMA because when you have a layer of silicon and you know the rate of etch selectivity then you know how much PMMA you need. We can see that the problem that the as the power increases the higher rate the PMMA etches.

Using SF_6 300sccm at 20C of 2,2Pa for 20s, changing the power from 10watt to 40watts at interval of 10watts.

Power (W)	10	20	40
Time (s)	20	20	20
PMMA_before_RIE (nm)	106,4549	164,535	162,5496
PMMA_after_RIE (nm)	69,5301	106,4549	66,6394
ΔRIE (nm)	36,9248	*58,0801*	95,9102
SIN_before_RIE (nm)	55,8345	75,2407	70,0454
SIN_after_RIE (nm)	43,8982	55,8345	42,1417
ΔRIE (nm)	11,9363	*19,4062*	27,9037

Power (W)	10	20	40
Time (s)	20	20	20
PMMA_before_RIE (nm)	224,193	242,6355	229,13
PMMA_after_RIE (nm)	164,535	164,5845	95,2674
ΔRIE (nm)	59,6582	*78,051*	133,8626
SIN_before_RIE (nm)	95,0723	94,9394	94,8491
SIN_after_RIE (nm)	74,9812	69,5822	59,9548
ΔRIE (nm)	20,0911	*25,3572*	34,8943

Table 4, selectivity, left to right, with thermal paste and without respectively

From the table above it can be seen that as the bias power is increased the selectivity SiN over PMMA decreases, for example at 10W the rate of PMMA decrease 34% faster compare to SiN.

6.2. Optimization

The objective of this section is to make holes in the SiN membrane in the shape of squares with dimension of 210nmx180nm, to form a matrix of 50x50 in a working area of $18\mu m\ X\ 18\mu m$. Transforming the above pattern into silicon nitride can be affected by many factors, hence a systematic approach is done to carefully test in order to optimize the transformation of patterns into the silicon nitride.

6.2.1 PMMA for pattern transformation

As discussed earlier PMMA is used as positive ton electron resist, in this setup a layer of PMMA 450 PMMA A-4 is spun on with 7000rpm for 45s, where the stencil is first mounted on the double tape and then place on the chuck that hold the silicon substrate 10x10, to ensure that the suspended membrane do not sag, otherwise the coated PMMA layer would not be uniformed and the silicon substrate can prevent the thin membrane to be pulled by vacuum under it. The membrane is prebaked on hot at 200C for 90s, followed by electron beam lithography, where the predefined design/pattern is written on PMMA (refer to Appendix p. after performing the EBL PMMA was developed in MIBK:IPA developer followed by stopper and rinsed with ISO-propanol followed by DI – water. The membrane was place on hot plate of 100C for 1 min to evaporate excess solvents and after inspecting with optical microscope 5xmagnification the patterns seems to be developed properly

To transform the pattern from the PMMA into 100nm Silicon Nitride membrane, reactive ion etching has been performed for 122s, which is the time required to etch 100nm SiN at 80watts, 20C using CF_6 gas

In this part same setup configuration is used where the etching power is lowered to 60, 40 and 30 watts respectively, after examining under optical microscope the membranes were completely etch away after RIE. Again the all procedure above is conducted in order to make that there were no systematic error involved, however the results obtain were the same as before where the whole membrane was etched away.

Figure 10. (a) After metal deposition, (b) after RIE

6.2.2 Aluminum as sacrificial mask

Dry etching is used due to its anisotropic etch, in other words the etching is performed unidirectional which is important for the formation of the desired pattern. In this section Aluminum is used as a sacrificial mask. To etch Aluminum $Cl_2, CCl_4, SiCl_4 BCl_3$ are needed [22]. Since SF_6 gas is used as plasma etchant in this project it would probably not affect the Aluminum in RIE process. In order to conduct a reasonable experiment a systematic approach has been taken where the Aluminum is tested in RIE to make sure that Aluminum stays intact under RIE After inspection with AFM no degradation on the aluminum thickness has been observed.

As it has been demonstrated before that PMMA cannot serve to transform the pattern into Silicon Nitride using Reactive Ion Etching due that PMMA´s low durability, a layer of Aluminum is deposited using E-beam metal deposition. Aluminum would serve as a sacrificial mask layer to shield the patterned areas of PMMA during reactive ion etching (RIE), in which subsequently undergoes lift-off is used, the mask layer is used

6.2.3 Prebake optimization

Prebake apply, bake process also called post bake or softbake which involves drying the resist after spin coat by evaporating excess solvent, reducing the solvent allows the solvent content to stabilize the resist film [23]. By baking the resist majority of solvent is removed where the thickness is reduce, development properties change, adhesion improves.

In order to achieve a good pattern transformation into silicon nitride it is important to optimize both time and temperature of the Prebake. Performing prebake for 90s at 200C followed by EBL, metal deposition and RIE, crack lines were present on the Silicon Nitride membrane, the crack lines were assumed to be due thermal condition in prebake process, and hence a systematic test on time and temperature (table 5) has been conducted. And a comparative study after RIE on each sample has been done.

Table 5, pre-bake temperature and time

Time	Temperature	Sample nr
90s	200C	1
90s	180C	2
5min	180C	3
10min	100C	4
30min	150C	5
30min	170C (conventional oven)	6

In this part EBL is performed on 6 samples using the above prebake condition respectively, process and configuration for all samples were kept constants, whereas only the time and temperature of the prebake has changed for each samples in order to conduct a reasonable comparative analysis on the effect of prebake time and temperature variation on the formation of crack lines.

The following Fig. [11] shows how the membrane looks before PMMA coating, after PMMA coating, after baking and after EBL. At this stage all samples look alike where there is no crack visible on the membrane.

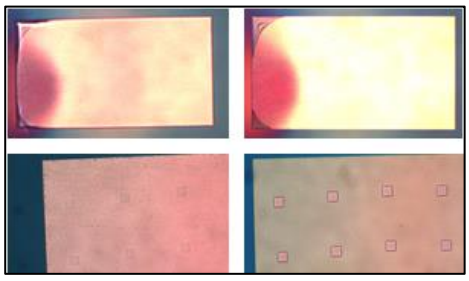


Figure 11(a) after PMMA coating
(b) after prebake (c) after EBL
(d) after development

Sample 1

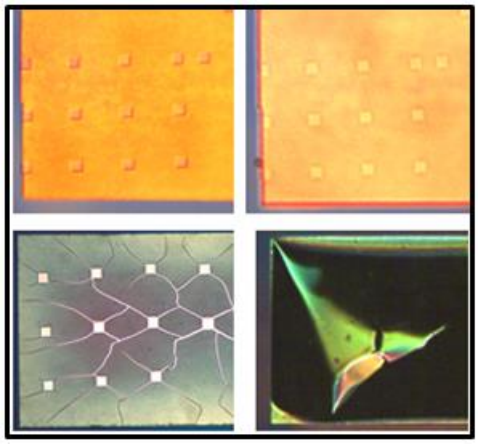


Figure 12 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

Sample 2

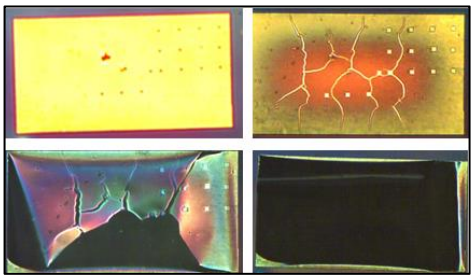


Figure 13 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

Sample 3

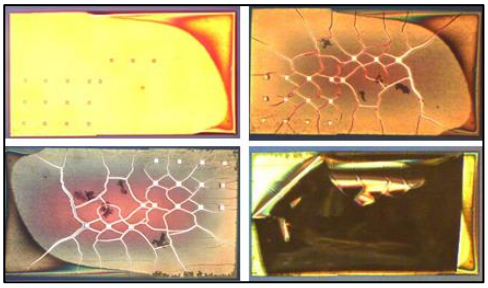


Figure 14 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

Sample 4

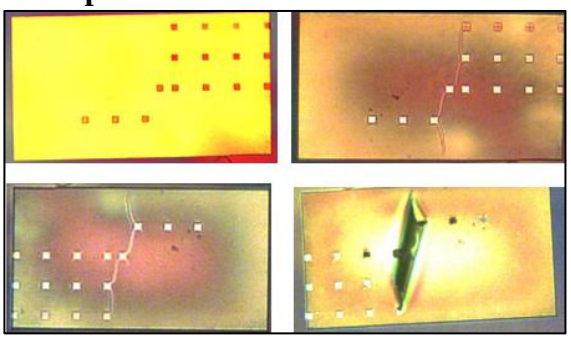


Figure 15 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

Sample 5

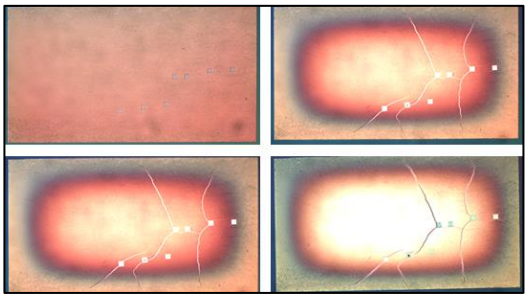


Figure 16 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

Sample 6

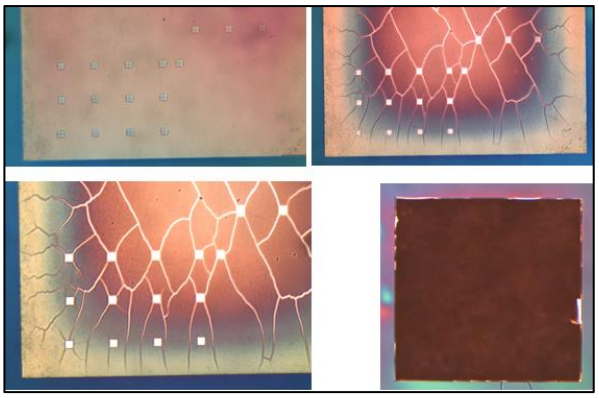


Figure 17 upper left; after metal deposition, upper right; after RIE, lower left; after second RIE, lower right; after 3rd RIE

6.2.4 Deposition optimization

In this section two factors is investigated; the angle of metal deposition and the rate of which the metal is deposited, in order to see if the mentioned factors has any influence on the formation of the cracks.

Tilt angle and metal deposition

It is important to protect the PMMA with a layer of Metal, for example Chrome or Aluminum. Due to safety issues in the clean room –Sønderborg only Aluminum is used for RIE, hence Aluminum is used in this project. The aim is to cover the PMMA pattern after EBL and development and not the Silicon Nitride. If the substrate is mounted on flat mounting disc, metal would be deposited both on PMMA and Silicon Nitride. This would cause problem when Reactive Ion Etching is performed Fig [18, a].

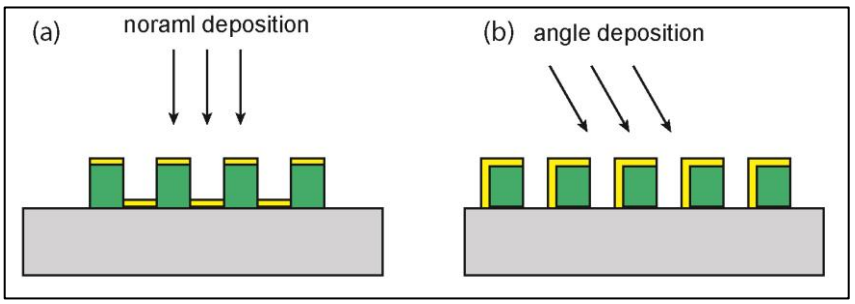


Figure 18, (a) normal deposition, (b) angle deposition

To deposit a layer of Aluminum on PMMA that has been developed, it is necessary to perform the deposition in a shallow angle. This avoids depositing metal on the SiN membrane, hence no etching would take place after reactive ion etching and to do that a substrate holder is made with two angles 60degrees and 70degrees, where the sample is mounted the placed in the deposition chamber upside down,

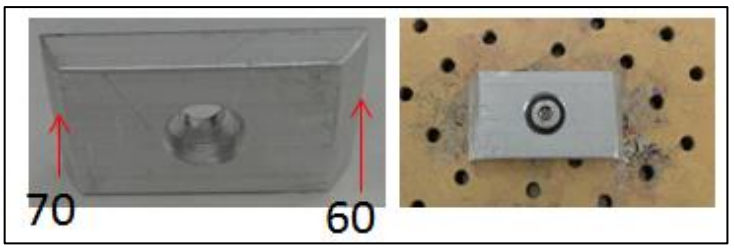


Figure 19, sample holder with 60 and 70 degree tilt

Setup

The stencil holder is first mounted on wafer carrier and then a double sided tape is mounted on tilt angle of the stencil holder, the stencil is carefully positioned upside down in the CRYOFOX transfer chamber for metal deposition shown in Fig.

Figure 20,sample holder

.

Two samples are tested with different angles in order to compare the results of the Aluminum layer on the PMMA and its effect on the SiN membrane after reactive ion etching.

The samples are pre-baked at 150C for 30min, where EBL is performed followed by development and 40nm of Aluminum is deposited with two angle setup. The samples are mounted on 60 degree and 70degree tilt respectively. After Reactive Ion Etching for 122s at 20C of 10watts, Lift-off process has been performed by soaking the samples in Acetone for 5min.

The pattern dimension was 210nmx180nm, where the width of the design is compared at different deposition angle. From the SEM image it can be seen that if the deposition angle is 60 degrees

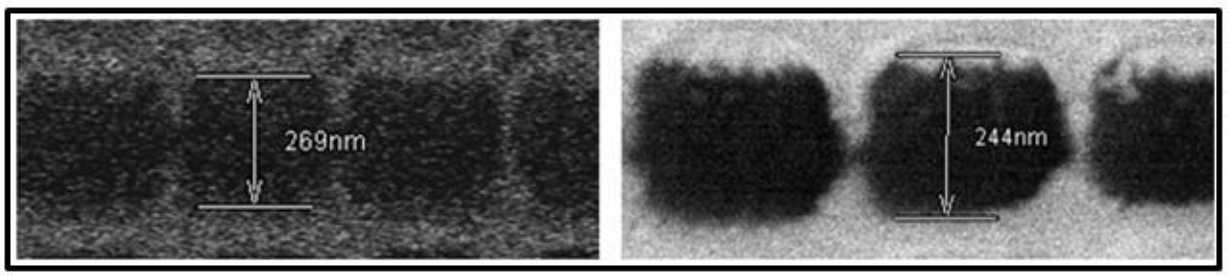


Figure 21, SEM image 60degree and 70 degree, left to right respectively

Another disadvantage of 60degree tilt angle is that after RIE the PMMA is etched away beneath the Aluminum layer, shown in Fig. [22]

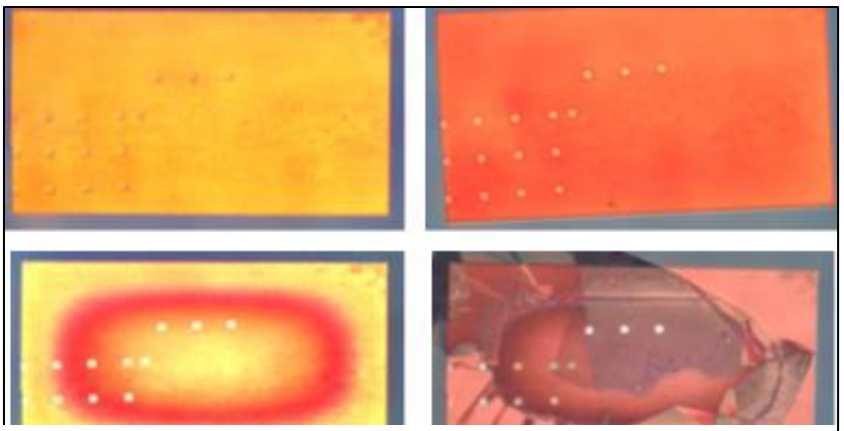


Figure 22 upper left, after EBL; upper right, after development, lower left after reactive ion etching, lower right , after liftoff and MF 311

Deposition rate and thickness

In this section two deposition rates are comparatively tested in order to see its effect on the formation of the cracks on the surface of the membrane. The same setup as before has been used for EBL and RIE where 40nm aluminum is deposited at 70 degree tilt with 0,5A/s and 1 A/s deposition rate

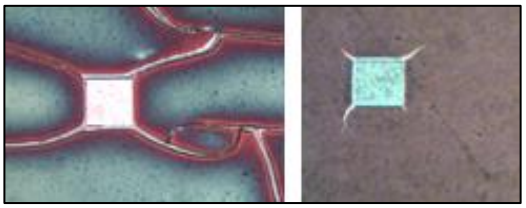


Figure 23 (a) 0, 5 A/s deposition rate, (b) 1A/s deposition rate

From the 100x magnification of the optical microscope image it can be seen that a deposition with lower rate has an effect on the formation of crack lines. This can be explained due the exposure of the membrane in the CRYOFOX metal deposition chamber. The heat from the e-beam causes the crack lines. Hence it is advisable to use a thinner Aluminum layer with high deposition rate, to avoid long exposure to the e-beam inside the deposition chamber.

Both samples are prebaked at 180C for 90s and etch with 10w at 20C for 100s only in order to keep the membrane intact for inspection. Ideally it should be etch for 122s to etch all the way in the SiN,, but due the presence of the cracks essentially on the PMMA which after 122s the membrane collapses as it cannot withstand its own weight. From the results of deposition it is clear that the longer time the membrane is exposed to e-beam metal deposition the more crack formation; hence it is a good idea to coat the PMMA with a high deposition rate and thinner layer of Aluminum.

Using MF 322

It is also known as Micro posits MF-322 developer Tetramethylammonium hydroxide, which removes aluminum layer in E-beam lithography. From series of experiments it is advisable if a thick layer of Aluminum is used; the n Aluminum should be removed using MF322 before Lift-off.

It has been experimentally determined to remove 14nm of Aluminum from SiN layer the substrate should be merged into the Micro posit MF-322 developer solution for 30seconds, followed by rinse with acetone, Isopropanol and DI-water.

Figure 24, MF 322 setup

6.2.5 RIE optimization

In the following section a systematic approach is conducted in order to optimize RIE of SiN membrane, where each factor is tested at a time and keeping other factors constant. This would allow reaching a clear conclusion, hence optimizing the recipe for fabrication of pattern on the SiN membrane.

6.2.6 RIE power

As the power increases the reaction increases hence the etching rate, the following table demonstrates how the thickness of the SiN changes as etching power is increased.

Table 6, etching power and SiN thickness

Power (W)	10	20	40
Time (s)	20	20	20
SIN_before_RIE (nm)	95,0723	94,9394	94,8491
SIN_after_RIE (nm)	74,9812	69,5822	59,9548
ΔRIE (nm)	20,0911	25,3572	34,8943

It is therefore reasonable to conduct the etching at 10W, in order to keep the surface temperature of the membrane low. Because as the power increases the reaction is faster hence the temperature due to the reaction increase, hence it is chosen to conduct the etching at 10W. further fore the etching rate of SiN is determined at 10W and 20C

6.2.7 RIE temperature

In order to see if the crack lines on the surface of the membrane is due to RIE temperature, two sets of experiments has been conducted, one where the sample was prebaked at 180C for 90s followed by EBL. 20nm of Aluminum is deposited with a tilt angle of 70 degrees at a rate of 1 A/s. RIE was performed at 10C for 122s with 10watts of power was followed Fig. [25] and the other sample was tested using the same setup above, only the RIE temperature was set to zero degrees Fig[26]

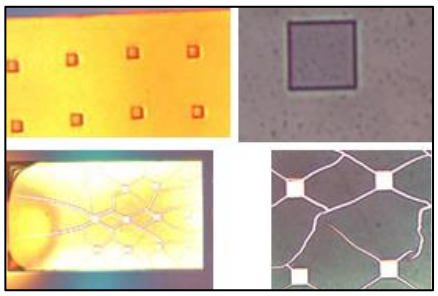


Figure 25Upper left, after Al deposition. Upper right, after Al deposition 20x magnification. Lower left, after RIE. Lower right, after RIE 20x magnification.

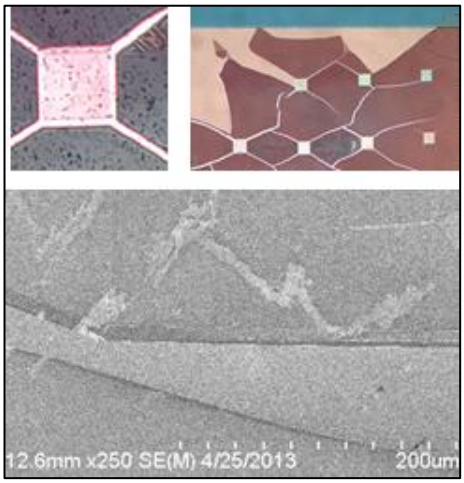


Figure 26upper left, single pattern after RIE. Upper right, after lift off. Lower, SEM image.

6.2.8 RIE time

It has been calculated that the required time to etch 100nm Silicon Nitride at 20C is 122s

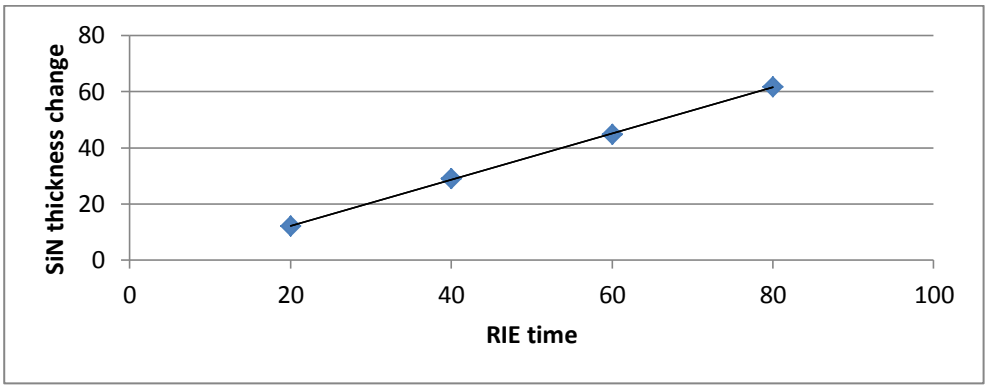


Figure 27 RIE time

The graph above represents SiN thickness changing in RIE over time (y = 0,8229x - 4, 3467) and (R^2 = 0, 9998)

The thickness of SiN were measured at various time interval, result is shown in Figure 2.

The slope from the graph represents the rate of SiN which is 0,8229nm/s, meaning that every second the SiN membrane is etched away 0,8229nm at (10W and 20C)

Etch time through 100nm SiN membrane required = $\frac{100nm}{0{,}8229nms^{-1}} = \mathbf{122}\boldsymbol{s}$

7. Stencil Characterization

In first part of this section after fabrication of stencil following the recipe from section 5.2 the stencil holes are characterized using SEM followed by the another section where the stencil is used to deposit 50nm of gold through on a silicon substrate and then characterized by SEM.

7.1 SEM inspection

Following the recipe from section 5.2, dose factor 2- 11 is tested, after REI only dose factors from 7-11 are survived shown bellow Fig[28] and Fig. [29]

Figure 28, 50x50 pattern with 7/8/9/ and 10 dose factor left to right respectively

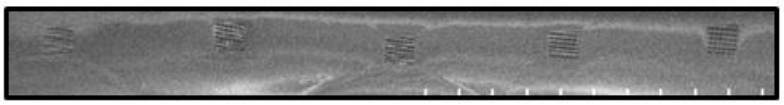


Figure 29, SEM image of dose factor 7-11

From section 6.1.3 it was clear that dose factor 4.8 would give a reasonable result, having dose factors from 7-11 available only, it worth inspecting with SEM to observe if increasing the dose lead to larger exposure , which result bigger holes in the stencil.

Setup

Each 50x50 pattern of 210nmX180nm at dose 7-11 is inspected by SEM, at coordinate 20, 10 for Height and 20, 12 for the Width shown in Fig.[30

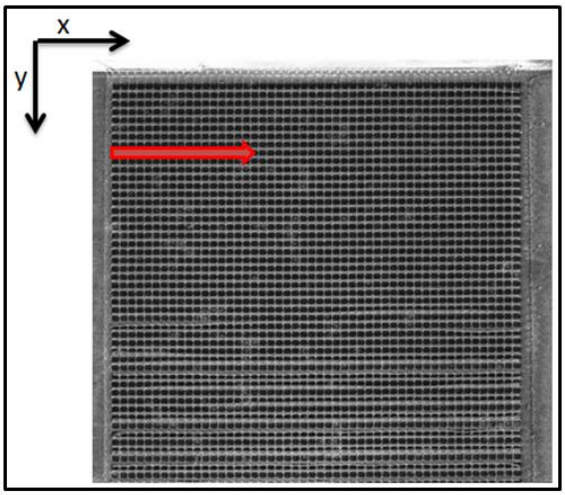


Figure 30, 50X50 pattern

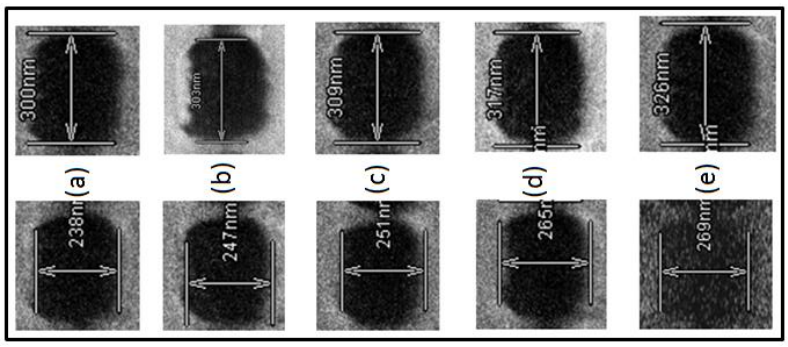


Figure 31, (a) dose 7, (b) dose 8, (c) dose 9, (d) dose10 (e) dose 11

a) 300nm X 238nm
b) 303nm X 247nm
c) 309nm X 251nm
d) 317nm X 265nm
e) 326nm X 269nm

It can be seen that the higher the dose the larger the stencil holes gets.

Crack lines on the surface of the Silicon nitride membrane

The reason that the Stencil cannot hold is due to formation of crack lines on the surface of membrane which is about 4,4um shown in Fig

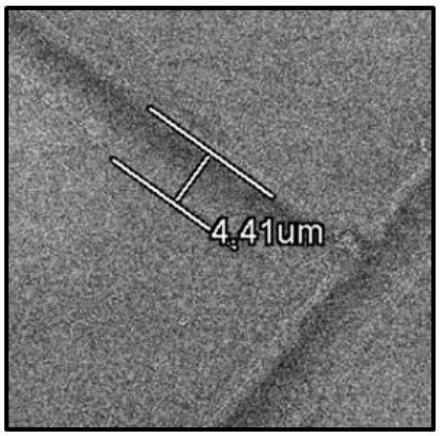


Figure 32,crack lines on SiN membrane

Further metal deposition on this stencil could not be performed in on this sample due to broken membrane

7.2 Metal deposition through Stencil

Recipe from section 5.2 has been used and only dose factor 5.5 has survived after RIE and liftoff.

Setup

After performing liftoff, the stencil is mounted on 5mmX5mm silicon substrate which is mounted on a double sided tape on wafer carrier. 5nm of Ti and 50nm of Au is deposited through the stencil at rate of 0,5 A/s and 1A/s respectively.

Figure 33, stenil on Silicon substrate for metal deposition

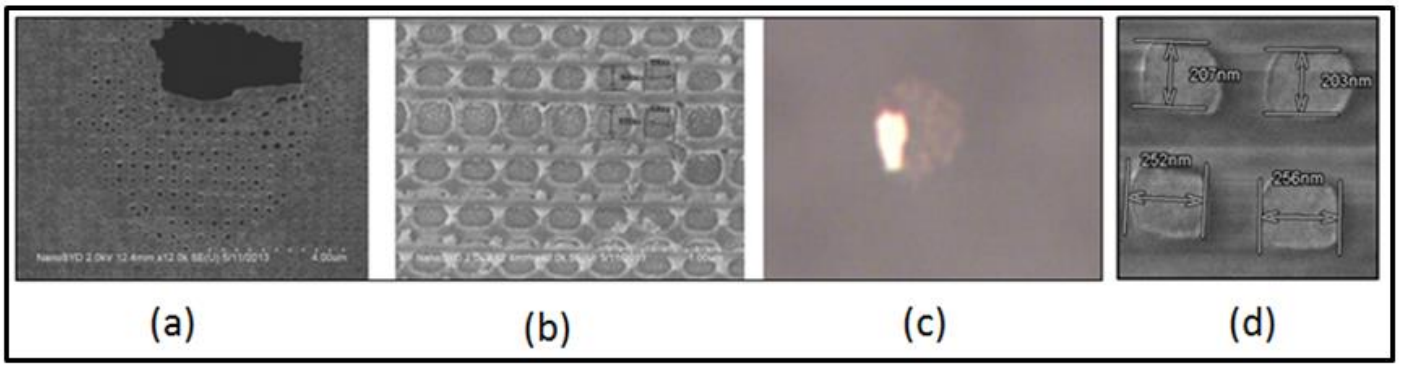


Figure 34, (a), (b) SEM image after RIE, (c) Optical microscope image 100 x magnifications after metal deposition on silicon substrate, (d) single SEM dimension after metal deposition

8. Interpretation

The results from DOSE test on 100nm silicon nitride and 300nm silicon nitride membrane shows that there is no difference in dimension using the same dose Fig [6]. This is due that there is no significant difference in the silicon nitride membrane, hence there would be not much difference in backscattering electrons from the membrane. as a result the dose test on 100nm or 300nm silicon nitride membrane DOSE not have any different, however the dose test on silicon substrate is significantly lower, this is because of the large thickness of silicon that produced a lot of backscattering electrons compare to thin silicon nitride membrane Fig. [6.d]. the argument above can be confirmed by comparing the results, that for silicon a dose factor of 1.8 and for 100nm silicon nitride membrane a dose factor of 4.8 is required. This means that more exposure is required for silicon nitride due to less backscattering compare to the silicon.

The results from Fig[9] shows that the etching rate of PMMA increase linearly, we can see from the graph that after 60s etching time about 166nm of PMMA is etched away, the result does not show a promising solution for pattern transformation from PMMA into silicon nitride, since to etch 100nm silicon nitride 122s is required Fig.[27]. For protection of PMMA a 30nm of Aluminum shows a good result, where RIE does not have any effect on etching the Aluminum.

It can be seen from Fig. [26] that there are no cracks on the stencil itself but the membrane, whereas the cracks were present not only on the membrane but also the stencil holder (silicon) itself. The cracks on the membrane still remain after RIE of $0°C$

Silicon has a good thermal conductivity of 149 $W{\cdot}m^{-1}{\cdot}K^{-1}$,[24] whereas Silicon Nitride has only 13 $W{\cdot}m^{-1}{\cdot}K^{-1}$ meaning that silicon conducts the heat faster compare to the silicon nitride. Silicon is placed on the carrier wafer using thermal past, the heat that is created under RIE would be conducted from silicon to the carrier wafer and further by Helium flow. On the other hand silicon nitride has a low thermal conductivity, leading the membrane to crack due to thermal stress on the surface of the silicon nitride. It can be concluded that decreasing the RIE temperature by $20°C$ improves the cracks on the silicon surface, but not the membrane itself.

More test could be conducted with different subzero temperatures, but throughout this project 10C etching temperature has been chosen.

Sample 5, Fig [16] shows a better result compare to sample 1-4 and 6. It can be said that the formation of the crack lines is less in lower temperature and longer time.

The tilt angle does not affect the formation of the crack lines but there is another problem can be seen from Fig. [22] That if the angle is lower than 70 degrees the PMMA etches away beneath the Aluminum layer, and from Fig. [21] it can be seen that the higher lower the angle the more metal is deposited on patterned PMMA.

From the SEM image comparison it can be said that it is reasonable to use a shallow angle of 70 degrees compare to 60degrees.

From Fig. [34] it can be seen that the stencil can be used for metal deposition if the crack lines does not occur,

Cracks vs Stress

When PMMA is hotter it possesses lower viscosity, and during the liquid phase there is no tension build up. It is not the stress that causes the cracks, rather when the PMMA is solidifies after prebake. During the hot plate or oven, there is no stress at all, when the polymer is cooled down, the stress rises. The solidification causes the stress that leads to the formation of the cracks.

From the experiments it can be seen that the cracks appear after Reactive Ion Etching, this means that the cracks should be present before the RIE, and the process that potentially would cause the cracks might be during the prebake, especially when PMMA is solidifies. Once the RIE is conducted, since there are cracks on the PMMA which later metal is deposited, the crack lines get etch into the membrane itself.

If the film was strained, the cracks form and regardless of parameter optimization on RIE, the cracks would simply be transferred into the membrane, as we observed from section 6.2.7 that changing the RIE temperature from 20C to 0C does not change the formation of the crack lines on the surface of the membrane.

9. Discussions

Dose test

Performing EBL, it is important to know how much each pattern should be exposed to e-beam in order to achieve a desirable result. The reason for the Dose test was conduction on a silicon substrate was to find out the correct DOSE factor for both silicon substrate (that could be used for later references) and silicon nitride membrane. Testing the different DOSE factors allowed to self-thought and practices the usage of SEM and CRYOFOX. A good amount of time has been spent in this part in order to completely get the hold of how to use the SEM, since there are many parameters to be taken under consideration when performing an EBL.

Etch rate measurements

For finding the etch rate of PMMA, Ellipsometer is used; where the height difference before and after the Reactive Ion Etching is measured by varied the time An alternative method could also be used where a layer of PMMA is spun at 7000rpm followed by EBL. After development 40s and 30 in developer and stopper respectively the height of the pattern can be measured with AFM. Then etching for 60s the height of the pattern is again measured with AFM. Finally the whole PMMA is etched away and the height difference is measured with AFM, having an exact height difference before and after the reactive ion etching the rate can be deduced since the RIE time is known (60s). This setup results a very precise etch rate compare to the setup using Ellipsometer, but due it time consuming the first setup is preferred.

SEM inspection of Membrane

Since Silicon Nitride membrane is only 100nm, hence the secondary electron which is the signal of interest is very low, but to improve this tilting the membrane around 20deg could improve the image quality, due to the fact that secondary electron is produced.

Sacrificial mask

As we can see from selectivity test using PMMA for pattern the transformation cannot be a reliable candidate, hence a layer of Aluminum is deposited to protect the PMMA. Other metals such as Chrome can also be used for PMMA protection, but due to technical issues only Aluminum is allowed to be used in ICP RIE (Sønderborg clean-room).

Prebake

When PMMA is spin coated on Silicon Nitride, it is important to keep the substrate level during transportation, as the PMMA is still in liquid form and any tilt would cause inhomogeneous layer. Before performing EBL on PMMA, prebake is necessary to anneal and density the PMMA film in order to remove voids within the polymer, in other words Pre bake serves two purposes: first, the solvent is removed by evaporation; second, it anneals the PMMA film.

It can be argued that PMMA spun at 7000rpm which result a thickness of around 160nm, would be thick which means that the solvent cannot completely evaporated, and when the sample is baked at high temperature may lead to solvent boiling that may result damage on the film. An alternative might be to use thinner PMMA layer or perform the baking process in two steps: baking at lower temperature to drive off the solvent and in the second step bake at 180°C to anneal and promote adhesion [31]

Hotplate Vs. conventional Oven

The formation of the crack lines on the membrane is the same wither the PMMA. It is prebaked on hotplate at 180C for 90s or in conventional oven for 170C for 30s. it can be discussed that the temperature is responsible compare to the time of the pre-bake when baked at high temperature all casting solvent gets completely removed and in the high temperature the PMMA gets thinned down, hence it would be worth investigating how does the temperature affect the membrane in terms of surface tension. Considering the fact that from the experiments it can be seen that the higher the temperature, the more tension would be created on the surface when it is developed the cracks would form. This is an analogue to macro word, for example, when a sheet of glass is drilled cracks form on the edges of the hole; this is due the uneven distribution of the tension on the surface. We can see the same phenomena on the corner of each pattern, where the cracks are generally initiated.

Time between EBL and Development

It has been observed that a delay after lithography decreases the image contrast, this was accidentally learnt, when a substrate was developed after 8 days and the dimensions were by 13nm smaller compare to a freshly developed substrate.

10. Future projects

Due to the limitation of time the following topics have not been investigated; but they are worthy of Further investigation and improvement in future projects.

10.1Thermal Simulation (COMSOLl)

Silicon has a good thermal conductivity of 149 $W \cdot m^{-1} \cdot K^{-1,}$ [26] whereas Silicon Nitride and PMMA has 13 $W \cdot m^{-1} \cdot K^{-1}$ of PMMA is0.5 $W \cdot m^{-1} \cdot K^{-1}$, thermal conductivity respectively and the formation of crack lines arises due to thermal stress on PMMA, when RIE is performed the cracks transfers to the membrane. To understand the how the crack lines arises due to temperature variation, one should simulate the stencil with a layer of PMMA, where the simulation is conducted on different temperature and characterize the surface.

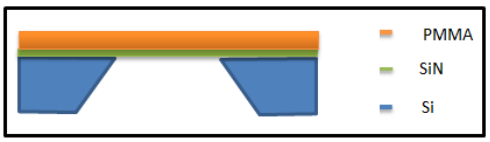


Figure 35. stencil

10.2 Subzero-degree temperature development

The surface tension is lowered if PMMA is developed at subzero temperature [27]

Development of PMMA should be optimized, where the membrane is tested in different temperatures after EBL in order to study the effect of the developer temperature on the formation of the crack lines on the surface of silicon membrane.

Cold development experiment setup

Developing the patterns after ELB using cold development, has shown significant difference on resist surface quality compare to normal room temperature development.[28]

Perform EBL on SiN membrane using 950 PMMA A4 as an e-beam resist spun at 7000rpm and develop at 1room temperature, 0C, -5C and -10C. Rinse the substrate with ISO – Propanol followed by DI-water. To investigate the formation of the crack lines on the SiN membrane, deposit 30nm of Gold to protect the PMMA from e-beam exposure when inspecting the membrane.

Presumably cold development might not help the formation of the cracks. Because as the film gets cooled down, it shrink and that increases the stress on the surface, more stress may be formed, but it worth investigate this factor.

10.3 Reusability of stencil

The life time of the Nano stencil is reduced due to clogging effect, it occurs when evaporated material, i.e. Gold particles accumulates on the stencil membrane and inside the apertures. This is very critical for the aperture because its shape get changed during the deposition process; the more the stencil is used the more it gets blocked.

-50x50 in on corner = 2500 holes total, ideally all holes would have the same dimension. Principally if one measures all 2500 holes and measures the diameter of them all; let's say if we perform metal deposition on substrate number 2, in reality there would be a variation because it practice a 100% reduced cannot be done, so the question is if there is a variation where in one region the holes are bigger compare to other region. If we do deposition on substrate nr.1 (make a SEM) and then deposit on substrate nr 2 (make a SEM) and do for substrate nr 3 -10 and see what happened as we increased the usage of each stencil. What is important is to take the SEM of the same region and compare it with the rest of the substrates, in this we eliminate error reading. This would result a poor conclusion. So to avoid this we could take a picture of the 3x3 of each right bottom of each block and compare it to other substrates. This allows comparing the same holes each time.

Reusability of Stencil experiment setup:

A systematic observation should be conducted on each corner and compare the corresponding after each use. It is important to compare the same pattern dimension after each use because there might be some factors that play a role at each corner , for example due to the gap between the stencil and the substrate different dimension may result.

Depositing 50nm gold on a silicon substrate

- Using AFM and SEM on the substrate for characterization

SEM on the stencil (AFM is not necessary because the height of the stencil is not interested, we only need to measure the diameter of the membrane opening)

This procedure should be repeated for each substrate,

Note: keep them in order for later use, where linear reflection spectroscopy should be used to characterize the reflectivity of the particles.

Tests:

- -deposition number1

-depositing 50nm gold through Nano-stencil

- Measure with AFM and SEM on the deposited particles

- take AFM picture of the stencil, this is to see how big the holes in the membrane are. This is important because when performing metal deposition, some of the metal would sit on the edges of the membrane hole, blocking the holes which are known as clogging effect.

- deposition number 2:

Measure AFM and SEM on the particles on the substrate and measure SEM on the Nano- stencil

- deposition number 3:

Repeat the process above.

10.4 Reflection spectra

A consecutive deposition using the same mask the reflection spectra of the gold particles using the Nano stencil is compared.

Averaging effect problem

Different stencil size result a different field effect hence it is important to compare the same dimension after consecutive deposition und reflection microscope. If the particle dimension is not the same then the result would be an average of absorption rater the exact spectra from each dimension, which makes it difficult to draw a rigid conclusion.

10.5 Self- assembled monolayers

Perform experiment 1 using self-assembled monolayer [29] and study the effect of using self-assembled monolayer and not using.

Simple just by dipping the clogged stencil in the ANP solution for 20 min [30]

10.6 Blurring

Blurring is one of SL challenges to be tackled and it arises due to the gap between the stencil and the substrate and factors that worth be investigates are; stencil to source gap, aperture size, deposition rate, substrate temperature.

10.7 Tempering

Tempering is a heating treatment is used to reduce some of the excess hardness. For example when molten glass is solidifies instantly; as it cools it pulls itself apart. To overcome this problem, the glass should be put in another oven where it is slowly cooled down; it will give the molecules time to find their relaxed position before it solidifies. Using this technique, one can apply after prebake, where the polymer is slowly cooled down. For example in case of 150C for 30 min prebake time, one can cool it down slowly for a quit longer time (30min).

10.8 spin coat in small islands

To reduce the formation of the crack lines on could spin coat PMMA in small regions (islands) because each one would shrink less away from each other. To address the problem with this method then PMMA should be spin coated in different step, where it gives expansion gap and allows the PMMA to shrink a little bit. This is how railway tracks and bridges are designed with a small gap between them so it there is a room for shrinkage for any temperature changes. Alternatively one could cover the rest of the stencil with a mask, where only PMMA is spin coated on the region of interest. Because when PMMA is spin coated, it covers the whole stencil 5mX5mm where the membrane is only in the region of 300um X 500um, and when it shrinks after prebakes during the cooling, the whole PMMA surface shrinks. If the area of interest is separated out, where there is no PMMA apart from where EBL is performed, it reduces the overall shrinkage.

11. Conclusion and outlook

This project can be summarized and concluded with an optimized recipe for pattern transformation into low stress silicon nitride (described in section 5.2).

The pattern designed by EBL successfully transferred into silicon membrane, where Gold was evaporated through the stencil but due to the formation of crack lines the stencil cannot be used for multiple metal depositions, hence the project could not be carried out further. The formation of crack lines are not completely eliminated, but significantly minimized if the substrate is pre-baked at 150C for 30min. however using hot plate vs. convention oven at higher temperature does not shows any difference, rather if the substrate is pre-baked.

It could be any combination to change the parameters, whenever we have thin films there is always problems associated with the tension and stress in them. But generally to work out the stress is annealing because slow cooling after prebake probably help to release the tension, therefore no formation of crack lines on the membrane.

High temperature is required to help the solvent to evaporate completely, but in case of the thin membrane the cracks occur on the surface, one could perform prebaking in two steps baking at lower temperature to drive off the solvent and in the second step bake at 180°C to anneal and promote adhesion. Sub-zero development was one of the factors that might affect the formation of crack lines; this could be tested along with other factors mentioned in future projects.

Another method to observe the formation of the cracks, one could use the polarize light to see the stress fields on the surface of the film before and after the prebake.

If more time would have been available the optical properties of the particles that were written directly on silicon substrate and the multiple usage of the stencil could be compared. The optical resonance from the direct EBL and stenciling could be comparatively shown in a graph, where wavelength and absorption can be drawn, and on the other hand the membrane after development could be coated with a layer of Gold to inspect with SEM.

12. Bibliography

[1] http://nanodevices.nl/facilities/equipment/123-raith-e-line-ebl.html

[2] http://nanolithography.gatech.edu/proximity.htm

[3] http://www.google.dk/imgres?imgurl=http://www.purdue.edu/rem/rs/graphics/sem2.

[4] Ozbay, E. "Plasmonics: Merging Photonics and Electronics at Nanoscale Dimensions" Science, 311, 189-193 (2006).

[5] Aksu, S., Yanik, A., Adato, R., Artar, A., Huang, M., Altug, H., "High-throughput Nanofabrication of Plasmonic
Infrared NanoAntenna Arrays for Vibrational Nanospectroscopy", Nano Lett., 10 (7), pp 2511–2518 (2010).

[6] Lieber, C. M.; Wang, Z. L. *MRS Bulletin* **2007,** 32, (2), 99-108.

[7] http://lmis1.epfl.ch
[8] http://www.zurich.ibm.com/st/nanofabrication/nanopatterning.html

[9] Brugger, J.; Berenschot, J. W.; Kuiper, S.; Nijdam, W.; Otter, B.; Elwenspoek, M. *Microelectronic Engineering* **2000,** 53, (1-4), 403-405.

[10] Lee, J. W.; Ju, B. K.; Jang, J.; Yoon, Y. S.; Kim, J. K. *Journal of Materials Science* **2007,** 42, (3), 1026-1030

[11] Cojocaru, C.-V.; Harnagea, C.; Rosei, F.; Pignolet, A.; van den Boogaart, M. A. F.; Brugger, J. *Applied Physics Letters* **2005,** 86, (18), 183107.

[12] Speets, E. A.; Riele, P. T.; van den Boogaart, M. A. F.; Doeswijk, L. M.; Ravoo, B. J.; Rijnders, G.; Brugger, J.; Reinhoudt, D. N.; Blank, D. H. A. *Advanced Functional Materials* **2006,** 16, (10), 1337-1342.

[13] Sidler, K.; Vazquez-Mena, O.; Savu, V.; Villanueva, G.; van den Boogaart, M. A. F.; Brugger, J. *Microelectronic Engineering* **2008,** 85, (5-6), 1108-1111.

[14] Arcamone, J.; van den Boogaart, M. A. F.; Serra-Graells, F.; Hansen, S.; Brugger, J.; Torres, F.; Abadal, G.; Barniol, N.; Perez-Murano, F. *2006 International Electron Devices Meeting, Vols 1 and 2* **2006**, 250-253.

[15] Deshmukh, M. M.; Ralph, D. C.; Thomas, M.; Silcox, J. *Applied Physics Letters* **1999,** 75, (11), 1631-1633.

[16] Yan, X. M.; Contreras, A. M.; Koebel, M. M.; Liddle, J. A.; Somorjai, G. A. *Nano Lett.* **2005,** 5, (6), 1129-1134.

[17] ftp://ftp.eecs.umich.edu/people/grizzle/papers/JECS99.pdf

[18] http://en.wikipedia.org/wiki/Reactive-ion_etching

[19] http://en.wikipedia.org/wiki/Electron_beam_physical_vapor_deposition

[20] *Dhananjay S. Bodas, R. V. Dabhade, Sheetal J. Patil, S.* A. *Gangal'*
Department of Electronic Science,
University of Pune, Pune: 4 1 1 007
India

[21] http://en.wikipedia.org/wiki/Silicon_nitride

[22] Wolf, S.; R.N. Tauber (1986). *Silicon Processing for the VLSI Era: Volume 1 - Process Technology*. Lattice Press. p. 546. ISBN 0-961672-3-7

[23] http://www.lithoguru.com/scientist/lithobasics.html

[24] http://en.wikipedia.org/wiki/Silicon

[25] http://en.wikipedia.org/wiki/Silicon

[26] http://nanoscale.mntl.illinois.edu/Publications/publications/342.pdf

[27] http://www.utdallas.edu/~walter.hu/research/publications/Hu%20dissertation.pdf

[28] M. Kolbel, R.W. Tjerkstra, et al., NanoLetters 2 (2002) 1339–1343.

[29] www.elsevier.com/locate/mee

[30] http://www.ece.ualberta.ca/~rj/phd-thesis/lit1.html#tab:pmma-material-properties-2