Organic Light Emitting Transistors Optimized By Self-assembled Monolayers

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Preface

This thesis has been submitted to partially fulfill the requirements of obtaining the Msc. Eng. degree from the University of Southern Denmark (SDU). The work has been conducted at NanoSYD, Mads Clausen Institute of SDU in Sonderborg. The project has been supervised by Associate Professor Jakob Kjelstrup-Hansen and co-supervised by Xuhai Liu, a PhD student in the NanoSYD group headed by Professor Horst-Günter Rubahn.

During this project, I have received generous technical and spiritual support from the group members of NanoSYD. First of all, I would like to express my gratitude to my supervisor Jakob Kjelstrup-Hansen for his support in every aspect of the project, especially for fruitful scientific discussions. I like to thank Xuhai Liu for his tremendous support in the experimental aspect. Especially, Xuhai thoroughly introduces me the set-ups used in the project. I like to thank Luciana Tavares and Kasper Thilsing-Hansen for guidance in cleanroom fabrication and nanofiber growth and transfer.

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Chapter 1 Introduction

Over the past decades, organic semiconductors have growing interests to the community of science and the industry[1]. Tremendous efforts have been put into the development of organic material based devices. In comparison to inorganic materials, organic materials have the following attributes attractive for commercial applications: 1). low-cost manufacturing processes such as solvent casting; 2). flexibility which enables its compatibility with soft substrates; 3). simplicity in tuning electrical properties through chemical engineering[2-4].

Among the organic semiconductor devices, organic field-effect transistors (OFETs) and organic light emitting diodes (OLEDs) have been under extensive investigations due to their great potential in commercial products. Based on the above devices, plastic electric products will have great impact on our lives, such as flexible displays made from OLEDs[5] and solar panels integrated into buildings, cars, clothing and fabrics. Actually, displays based on OLEDs have been available in the market. OFETs are on the verge of commercialization[6].

In the work of this master project, the subject is organic light emitting transistors (OLETs), specifically p6P light emitting transistors (p6P LETs). Compared to an OLED, an organic light-emitting transistor (OLET) is more attractive due to its unique capability of integrating current modulation and light-emitting properties[7], thus being a promising platform for fabrication of novel optoelectronic devices such as large-area displays. Moreover, Raffaella Capelli and his co-worker have demonstrated that an OLET outperforms the equivalent LEDs with respect to efficiency[8].

For organic thin film transistors (OTFTs) with metal as electrodes, tunneling resistance at the metal (gold usually)/organic semiconductor interface has been identified as a bottleneck for charge transport and consequently energy efficiency[6]. One of the promising solutions for the problem is to apply self-assembled monolayers (SAMs) on the gold surface. SAMs on gold have been regarded as a convenient means for surface modification[9]. For the project, the aim is to improve current-voltage characteristics and light emission intensity of p6P FETs by SAMs.

This work is concerned with the opto/electrical performance of p6P FETs. Chapter 2 gives an introduction to p6P, general principles of light emitting transistors. Chapter 3 details fabrication

and experiments performed, with the results presented in chapter 4. Chapter 5 summarizes the conclusions and makes suggestions for future work.

Chapter 2 Basics of p6P and OFETs

For the project, the active organic semiconductor of OFETs is p6P. p6P is able to emit blue light through photoluminescence (PL) and electroluminescence (EL). More importantly, p6P molecules are able to assemble into 1-D nanostructures –nanofibers[11]. The light from a p6P nanofiber is highly anisotropic, polarized[12]. The properties make p6P a promising candidate as a functional material used in optical waveguides and light emitting devices[10]. The chapter is to give a brief review of p6P and p6P FETs and its problems.

2.1 Characteristics of p6P molecules, thin films and nanofibers

The para-hexaphenyl (p-6P, C36H26) molecule is an aromatic compound which consists of six phenyl rings connected in a para configuration as seen in Fig 2.1. The length of a single p6P molecule is 2.44 nm.



Fig 2.1 p-6P molecule

As an element in valance group IV, Carbon has electron orbital structure (1s)2(2s)2(2p)2 when isolated. To form the two-dimensional phenylene ring structure the electron orbital of Carbon hybridizes to (1s)2(sp2)3(2p), where two of the sp2 orbital (marked turquoise in Fig 2.2a) form strong σ -bonds between the Carbon atoms and the remaining sp2 orbital's bond to Hydrogen atoms. The $2p_z$ orbital (marked pink in Fig 2.2a) forms weak aromatic π -bond between the Carbon atoms and it is this weak aromatic π -bond which determines the Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO)[10]. The LUMO level and the HOMO level are analog to the conduction band and valence band in inorganic semiconductor.

p-6P is able to self-assemble into crystalline structures. The crystal structure p-6P is classified as a herringbone structure which is characterized by a large tilt angle between neighboring molecular planes[11]. This herringbone structure with a tilt angle of 66° and the unit cell of p-6P

can be seen in Fig. 2.2c. The monoclinic unit cell contains two p-6P molecules.



Fig 2.2: (a) A phenylene ring consist of six Carbon atoms bound together by strong σ -bonds (the Carbon sp2 hybrid atomic orbital) and weak aromatic π -bonds (the remaining Carbon p atomic orbital). (b) Para-hexaphenyl consists of six phenylene rings bound together in a linear chain by single σ -bonds. The aromatic π -bonds determine the HOMO and LUMO levels (here the HOMO level is shown). (c) p6P crystallizes in a herringbone structure with two molecules per unit cell [10].

At room temperature, p6P is solid. p6P can be sublimed and then form a nanoscaled thin film on a substrate, such as gold and silicon. The film is amorphous. However, when grown under the proper conditions, i.e. pressure, temperature and deposition rate, on a cleaved mica substrate, p6P forms nanofiberss which resembles small needles. The fibers are well aligned over a large area. The needles can have lengths up to 1 mm, widths up to 800nm, heights up to 200nm[12].



Fig 2.2 AFM image of 2 p6P fibers on muscovite mica

The band gap of p6P crystal is 3.1 ev (i.e. the energy difference between LUMO 2.9 ev and HOMO 6.0 ev[13]). Upon UV exposure, electrons at HOMO are excited to LUMO. After a short relaxation time, electrons jump back and recombine with holes at HOMO. The recombination emits a photon, whose energy is equal to the energy difference between the two orbitals. Due to its wide gap, p6P can emit blue light, which is essential for full-color displays. The fluorescent light from a p6P nanofiber is highly polarized. With a linear analyzer, the polarization is observed under a fluorescent microscope as shown in Fig 2.3.



Fig 2.3 Fluorescent microscope images of p6P fibers with different angles of Analyzer (red line)

2.2 Basics of OFETs

Organic thin film field effect transistors (OTFFETs) consist of 4 components-an organic semiconductor (OS) film, drain/source electrodes, dielectric, and a gate. According to the

geometry of the device, OTFFETs can be classified into 3 groups. For example, if drain/source electrodes and gate are both at the bottom of OS as shown in Fig 2.4, the configuration is called Bottom Contact/Bottom Gate (BC/BG). The other two configurations are Top Contact/Bottom Gate (TC/BG) and Bottom Contact/Top Gate (BC/TG). The configuration has effects on charge transport, morphologies of an organic film and trapping states[14], which are out of the scope of the project.



Fig 2.4 BC/BG structured OFET, with channel length L and width W.

The samples prepared for the project are all with the same configuration-BC/BG. The main reason is that BC/BG transistors are relatively easy to fabricate. For TC/BG configurations, stencils may be required to have patterned electrodes on an organic film, because p6P (as organic materials) are not compatible with photolithography (a standard pattern transfer technology in the semiconductor industry), which is used to pattern electrodes for BC/BG transistors.

Classified by the majority current carrier in a channel, transistors are grouped into 3 typesbipolar (both holes and electrons), p-type (holes) and n-type (electrons). The p6P FETs have ptype characteristics[16].

To model charge transport of a FET in a simplified way, it is assumed that source-dielectric-gate behaves like a capacitance with a threshold voltage V_{Th} . When Vg is below V_{Th} and Vd is unbiased, the capacitance is uncharged, which means no mobile charge. When Vg is above V_{Th} and Vd is unbiased, mobile charges at the unit area of source contact is[14] $Q_{mob} = C_i(Vg - V_{Th})$ Eq 2.1

where Ci is capacitance per unit area of source contact.

If the drain is biased to Vd, then at position x along the channel, Eq 2.1 is modified to

 $Q_{\text{mob}} = C_i (Vg - V_{\text{Th}} - V_{(x)}) \quad Eq \ 2.2$

In a perfect model, current leakage and diffusion current are nonexistent. Then the source/drain current is

 $I_{ds} = W \mu Q_{mob} E x$ Eq 2.3

Where W is the channel width, μ is carrier mobility, Ex is the electric field at the channel position x. Apply E=dV/dx and to Eq 2.3, then

 $I_{\text{ds}}\,dx = \mathscr{W}\!\mu C_{\text{i}} \big(Vg \text{ - } V_{\text{Th}} \text{ - } V_{(x)} \, \big) dV \quad Eq\,2.4$

Integrate Eq along x from 0 to L, and then we have

$$I_{ds} = \frac{W}{L} \mu C_i [(Vg - V_{Th}) V_d - \frac{1}{2} V_{ds^2}] \quad Eq 2.5$$

If $V_{ds} \ll Vg - V_{Th}$, then

$$I_{ds} = \frac{W}{L} \mu / in C_i (Vg - V_{Th}) V_{ds} \quad Eq \ 2.6$$

In this regime, Ids is proportional to Vds.

From Eq 2.5, we get the first derivative of Ids with respect to Vds

$$\frac{\mathrm{dI}_{\mathrm{ds}-}}{\mathrm{dV}_{\mathrm{ds}}} = \frac{\mathrm{W}}{\mathrm{L}} \,\mu \mathrm{C}_{\mathrm{i}}(\mathrm{Vg} - \mathrm{V}_{\mathrm{Th}} - \mathrm{V}_{\mathrm{ds}}) \qquad \mathrm{Eq} \, 2.7$$

When Vds is equal to Vg-VTh,

$$\frac{\mathrm{dI}_{\mathrm{ds}}}{\mathrm{dV}_{\mathrm{ds}}} = 0 \qquad \mathrm{Eq} \ 2.8$$

Ids reach an extreme, which is called saturated current.

$$I_{ds, sat} = \frac{W}{2L} \mu_{sat} C_i (Vg - V_{Th})^2 \qquad Eq \ 2.9$$

When Vds is more than $Vg-V_{Th}$, Ids does not increase any more, which is saturation regime. Physically, it means the channel is pinched-off near the drain electrode.



Fig 2.4 I-V plot of p-type FET model

2.3 Light emission of p6P FETs

The light emission mechanism of p6P FETs is not well understood yet. EL from thin film transistors is firstly observed from an OFET (but not a p6P FET) under AC -driving, instead of DC-driving[15]. In the article[16], a similar model has been proposed to describe EL of p6P under AC driving. During the light emission experiment, the drain/sources are grounded and the gate electrode is AC biased. Under this configuration, blue light is emitted as shown in Fig 2.5(a). The peak of EL spectra is reached around 430 nm. As seen in Fig 2.5 (b), the EL and PL of p6P have almost the same spectra features.



Fig 2.5 (a) Optical microscope image of the EL output of a 60 nm p6P thin film biased with Vds = 60 V and a sinusoidal gate voltage with an amplitude of 75 V and a frequency of 200 kHz (b) Normalized PL and EL spectra from a p6P thin film[16].

2.4 Problems and challenges

Despite p6P has great opto/electrical properties as functional materials, p6P based devices are far from maturity and have many problems. Stability over a long lifetime is not yet achieved[26]. Driving voltage is high-several tens of volts[16].

One of the reasons for high driving voltage is the existence of hole inject barrier (HIB) at the electrode/semiconductor interface, which is due to the mismatch between the work function of electrodes (Au 5.1 ev[17]) and the level of HOMO (6.0 ev) of p6P as depicted in Fig 2.7. In a

simple framework disregarding interface charges, the injection barrier for holes is $\Phi_B{}^h=0.9$ ev, for electrons $\Phi_B{}^e=2.2$ ev.

It has been reported that a SAM is able to increase or decrease work function of metal[18]. Consequently, the injection barrier for holes (or electrons) is tuned. For the case of p6P, the majority charge carriers are holes. For current-voltage characteristics, Φ_B^h is the concern. However, as mentioned in the above section, for light emission, both holes and electrons are injected. Therefore, both injection barriers are taken into account when it comes to light emission.



Fig 2.7 Illustrative energy diagram for describing HIB

Chapter 3 Sample Preparation and Experiment Detail

The preparation of samples includes cleanroom fabrication, SAMs coating and p6P thin film deposition and wire bonding. The Ids-Vds relationship and light emission intensity are measured. In the end of the chapter, the experimental design for the project is addressed.

3.1 FET substrate fabrication

The FET substrates are prepared in a cleanroom. The substrate consists of two main componentscomb finger-like drain/source electrodes on silicon oxide and a gate electrode deposited on ndoped silicon. Each substrate has 20 pairs of drain/source electrodes. The distance between the electrodes is 10um. The width is of a drain/source electrode finger is 50um. The length of a finger is 1.45 mm. Each substrate is 3mm wide, 5mm long. The structures are patterned via photolithography. The recipe is described in detail in Appendix-1.



Fig3.1 Disproportional image of a FET substrate

The wafer used in the project is 525 um thick with 300 nm silicon oxide. The fabrication flow consists of four steps as depicted in Fig 3.2. The first step is to pattern a gate window on oxide with photoresist. Then the wafer is immersed in HF solvent for 7 minutes. After that, exposed silicon oxide is etched away. The second step is to deposit metals via evaporation. A 2 nm Ti layer is deposited prior to 48 nm Au deposition to improve adhesion to the wafer. After lift-off in acetone, the gate electrode is ready. Thirdly, the drain/source electrode pattern is transferred from the corresponding mask. The last step is deposition and lift-off, which is the same with the second step. It shall be noted that the rough gold surface is bad for the quality of SAM coating. In order to have smooth gold surface, deposition rate is tuned to 0.02nm/s. In Fig 3.3, it is an

AFM image of gold surface. As an indication of the roughness, the root of mean square (RMS) of gold surface is calculated, which is 0.287 nm.



Fig 3.2 Brief processes of FET substrate fabrication



Fig 3.3 AFM image of gold surface

After the fabrication, it is checked if there is gold between electrodes and the gold surface is very smooth. After the quality is checked, the wafer is coated with 1.5 um thick photoresist. This is to avoid contaminants on substrate surface. Then the wafer is diced into chips.

3.2 Application of SAMs

Before coating SAMs, substrates are rinsed in acetone with sonic agitation for 1 minute to

remove photoresist, which is spin-coated on as a protection layer before wafer dicing. Then they are blown dry with stream of nitrogen. To avoid contaminants on gold surface, the samples are used less than an hour after being rinsed.

In order to verify the effect of coating, the substrates are divided into 3 groups. One group is untreated with SAMs. The samples of the other two groups are immersed in two different solvents for 24 hours, which is long enough to guarantee coverage density [23, 29]. The solution is the same-pure ethanol. The two solutes are 1H,1H,2H,2H-Perfluorodecanethiol (PFDT, $CF_3(CF_2)_7(CH_2)_2SH$) and Octadecyl mercaptan (OM, $CH_3(CH_2)_{17}SH$). The molar concentrations of both PFDT and OM are 1.75 mM.



Fig 3.4 PFDT and OM molecules and SAM dipole moment polarizations

OM is a kind of alkanethiol, and PFDT is perfluorinated alkanethiol. Both of alkanethiols and perfuorinated alkanethiol are known to form SAMs on gold. PFDT and OM have opposite polarizations of dipole moment. PFDT has positive parts near gold surface, OM negative[18]. The dipole of OM induces electrical field, whose component normal to the surface is negative (pointing towards to the interior of the surface). Consequently, the HIB will be higher. The PFDT works the opposite way.

When taken out of solvent, on the gold surface a monolayer of molecules is assembled. It is dissociative chemisorption. In another word, the S-H bond in the molecule is broken and S is

strongly bonded to Au on the surface.

The SAM is a highly ordered, ultra-thin, two-dimensional layer. The basic building block of the structure of an alkylthiolate SAM on Au(111) is well-known[19]. It consists of one thiolate molecule per $\sqrt{3} \times \sqrt{3}R30^{\circ}$ surface per unit cell. The molecule keep an approximate off-normal tilt of 30°, and between molecules, the nearest neighbour distance is 4.97 Å[21]. The structure of perfluorinated alkanethiol SAM is not concluded yet[19].



Fig 3.5 Schematic model of the $\sqrt{3} \times \sqrt{3}R30^{\circ}$ overlayer structure formed by alkanethiolate SAMs on Au(111) [20].

Besides chemisorpted monolayers, there are also physically absorbed molecules overlaid on monolayers. Therefore, the samples are rinsed thoroughly (over 5 minutes) in acetone. Rinsing only breaks physical adsorption. The chemisorpted monolayer remains intact. To offset the influence of rinsing, the reference group is also rinsed as coated ones. After rinsing, all samples are blown dry with nitrogen.

3.3 p6P deposition

The two groups with SAMs and the untreated group are coated with 30 nm p6P thin film via physical vapor deposition (PVD) in a vacuum chamber set-up. The working principle is that in Ultra-high vacuum (UHV), p6P is sublimed by an oven and then the p6P vapor is condensed on the FET substrate surface at room temperature. The system is made up of three main parts and accessories as shown in Fig 3.5. The three main parts are a two-stage pumping system, a transfer chamber and a deposition chamber.



Fig 3.5 Diagram of physical vapor deposition set-up

The p6P thin film deposition manual is included in Appendix-2. The setting for coating p6P thin film is as follows.

Oven supply: 2.2 A Oven temperature: 8.15V Deposition Pressure: 5.2e-8 mbar Rate: 0.3-0.2Å/second Thickness: 30 nm

3.4 Wire bonding

Samples are bonded to a chip substrate before light emission measurements. It is necessary because light emission is achieved in vacuum where the voltage is applied to the sample via a sample holder. The sample bonded to the chip substrate is clamped to the sample holder. The basic work procedure of a wire bonder is that at the first bonding point wire (silver in this case) is pressed on the specimen by a wedge and melted by sonic power, then the wedge is lifted and moved to the second bonding point and at there the wire is pressed, melted again and then cut off when the wedge is lifted again. The settings of the wire bonder are very critical to the quality of

bonding. The settings used for the project are as shown in Table 1.

	Power	Time	Force
1 st bonding point	3.7	4	3
2 nd bonding point	3.7	4	3

Table 1 Bonding parameters. Note that they are relative values without units from the machine.

3.5 Current-Voltage characterization

Current-Voltage characterization is done with a probe station, a LabVIEW program and two voltage amplifiers, an ampere meter and a DAQ (data acquisition) card.

The probe station has three probes which are positioned by 3-D micro-manipulators. The three probes contact the three electrodes of a sample. Over the sample is an optical microscope used for vision assistance. The lamp of the microscope is turned on when we try to get contacts with the sample. The illumination has effects on the performance of samples, which is discussed in section 4.1.1. Therefore, a box covers the inter-digital part of a sample, only leaving the electrode pads at the bottom exposed to light. The gate voltage and the drain/source biased voltage are applied via the three probes. The values of them are set by the LabVIEW program. The current (typically less than 1e-6A) is measured by a very sensitive meter, whose best sensitivity is 1e-15A. Then the value is sampled and sent to the LabVIEW program. The program is able to apply sweeping and stepped voltage and save/plot I-V data. The graphical user interface of the program has been included in Appendix-3.



Fig 3.6 Diagram of I-V measurement with probe station and equivalent circuit

3.6 Light emission experiment

The set-up of light emission experiment consists of three main parts. The first part is a vacuum chamber (vacuumed by a rough pump) and power supply for a sample. The sample is put in the vacuum chamber with the active part facing the glass window. All the samples are fixed at the same point. The power source is a function generator, whose signal is amplified 25 times before applied to the gate of the samples. Drain and source electrodes are grounded as shown in Fig 3.7.



Fig 3.7 Light emission intensity measurement set-up diagram



Fig 3.8 Equivalent circuit of light emission configuration

The second part is to collect the light from the sample and convert its intensity to voltage. A lens is placed in the front of the chamber window to collect the light from the sample. Then the collected light is linearly converted to current via a photon multiplier tube (PMT). The positions of PMT and objective are 3-D adjustable for collecting the light as much as possible. After adjustment, the positions are marked. Before each measurement, they are moved to the marked positions. By this way, the measurement of each sample is done under the same situation. Therefore, the results from different samples are comparable. The PMT is powered by a high voltage supplier. It is a very sensitive instrument. The output current of PMT increases with its power supply. In the project, the voltage is fixed at 1000V. The output is current, which is little (below 1e-6A). Therefore, a preamplifier (the purple block in Fig 3.7) is used. The amplifier is a low frequency pass filter. It can work at a narrow frequency width (20 kHz) or a wide frequency (1MHz) mode. The input signal from PMT is converted to voltage and amplified at the same time the preamplifier is voltage. It has three amplifying levels--1e5 V/A, 1e6 V/A, and 1e7 V/A. In the experiment, its frequency width is 20 kHz and its amplifying level 1e7 V/A.

The third part is a DAQ card and a LabVIEW program. The converted signal is sampled by the DAQ card. Sampled data are saved and plotted. Meanwhile, the program calculates the mean value and saves it into a text file. The graphical user interface of the program has been included as Appendix-4.

3.7 SAM thickness measurement

The thickness of a SAM on gold is measured by an ellipsometer. An ellipsometer is a sensitive optical technique. The set-up of an ellipsometry measurement is shown in Fig 3.9.



Fig 3.9 Schematic set-up of an ellipsometry measurement

In this technique, the complex reflectance ratio is measured as the right hand of Eq 3.1.

$$\rho = \frac{r_p}{r_s} = \tan(\psi)e^{i\Delta}$$
Eq 3.1

where r_p is the complex reflectivity for p-polarized light, r_s is for s-polarized light, $tan(\psi)$ is the amplitude ratio upon reflection and Δ is phase shift difference.

Specifically, it measures the ration between p-polarized and s-polarized complex reflectivity from the sample. And then the value is related to the properties of the sample (such as thickness or refractive index) by an optical model embedded in the instrument software.

Each measurement is able to two determine two variances at most. The variances are obtained by running simulation. Starting from approximated initial values assigned to them by users, the simulation keeps updating values of the variances until the updated values lead to best fit between simulated $tan(\psi)$ and Δ and measured $tan(\psi)$ and Δ .

The optical model, as shown in Fig 3.10, is applied to get the thickness of a SAM in the project. The thicknesses of a SAM and Au are to fit, while those of Ti and SiO2 are known. The substrate is Si. The corresponding optical parameters (refractive index-N and adsorption coefficient-K) for air, Au, Ti, SiO2 and Si are given in the standard library of the fitting software while the monolayer is defined by assigning values to N and K before simulation. The two monolayers

have same values, N=1.5 and K=0. After simulation with measured raw ellipsometry data and the model, a best-fit value of thickness of the SAM is obtained.



Fig 3.10 layer stack of a sample

3.8 Experimental design

The project is to improve p6P FET I-V characteristics and its light emission by SAMs. But the p6P light emitting thin film transistors were reported in July, 2010[16]. Not much has been done to document its I-V characteristics and light emission performance, such as reproducibility and stability over time, and degradation during operation. Therefore, it is desirable to have better understanding of p6P thin film transistors and identify the factors that contribute to their performance variances before working on optimization by the application of interface treatment. Several **reference groups** (the bold font is to distinguish them from the reference group used to compare the effect of SAMs.) of samples are prepared for this purpose. All the samples of each group are from the same wafer and coated p6P at the same time. They go through the same manufacturing processes. Therefore, the performance differences introduced by fabrication are avoided as much as possible. After work at the initial stage is done, three groups of samples are prepared to verify the optimization by SAMs.

Chapter 4 Results and Discussions

In this part, the results from **reference groups** are presented and discussed first, and then the improvements of p6P LETs achieved by SAMs are analyzed.

4.1.1 Current-Voltage characteristics of p6P FETs

In Fig 4.1, it is an I-V plot of p6P FET at different Vg with Vds sweeping. There is mismatch between the curve of Vds sweeping forward and that of Vds sweeping backward. The phenomenon is called hysteresis. The reason can be space charge at the metal/organic semiconductor interface and/or the organic semiconductor/dielectric interface[25].



Fig 4.1 Ids-Vds plot--Vds sweeping from 0 to -60, Vg stepping from 0 (deep red) to -45V (blue) with a 15V step length

Actually, it is hard to get p6P FETs working at the saturation regime. As seen in Fig 4.1, the driving voltage is high, but the saturation current is not achieved. Besides high contact resistance, the high driving voltage can be ascribed to the thickness of silicon oxide (300 nm) and the low mobility of current carriers (1e-6 cm²/Vs[16]). It is highly possible that the sample breaks down (due to high electrical field in the conductance chanel) before starting saturating if the bias between drain and source is raised further. Moreover, the yield is too low, less than 10%. These

make impossible to extract reliable standard specifications of p6P FETs such as V_{Th} and I_{sat} , which are averaged from significant quantity of samples[24]. Therefore, during the verification of SAM effects, the I-V measurement is simplified--sweeping Vds while the gate is grounded. By comparing Ids at a specific voltage, the effects of SAMs on I-V characteristics are still able to be checked.

In the beginning of the project, it was found that illumination from the optical microscope of the probe station has an effect on results during I-V measurements. When the bulb with the optical microscope is on during the measurement, a sample has higher current as shown in Fig 4.2 (left). When the bulb is on, the current at Vds=30V is over 4 times higher than that with the bulb off. It is suspected that light generates hole-electron pairs in p6P. Moreover, the effect of illumination lasts for 3 minutes at least after the bulb is turned off, which is like memory effect. The possible reason is that incandescent light conveys thermal energy to p6P. Consequently, the density of mobile charges is increased or the mobility of current carrier is increased. Measuring I-V characteristics under higher temperature (for example on a 35 °C hot plate) is able to disclose if the thermal energy is the reason for higher current. The photoconductivity and "memory effect" are interesting phenomena to investigate, but beyond the scope of the project. To avoid the illumination effect, the samples' upper part during positioning probes is covered.



Fig 4.2 Effects of illumination on conductivity, (left) plots of measurements with/without illumination, (right) off1-5 are corresponding to measurements done 1-5 minutes after lamp is off.

Before the project was started, it had been known that the I-V characteristics are different among samples. It was also observed that the I-V characteristic of a sample may different between two measurements. For example, the I-V characteristic is improved over time[26]. It was assumed that the improvement is due to self-crystalline of p6P. It is desirable to have narrow performance

variances among samples and stable samples over a long lifetime. Annealing is employed for this purpose. The idea is to accelerate the process of assumed self-crystalline processes of p6P after deposition, so that the stability of p6P over time is achieved. Two groups are prepared. After p6P deposition, all samples' I-V characteristics are measured. Then the first group is annealed through placing on a hot plate (80 °C) for 20 minutes and then cooling down in air. One hour after that, the second round measurement is carried on. Four days after annealing, the final round is completed. The results are plotted in Fig 4.3. From the reference group, the improvement over time is observed, which agrees with the observation in the literature[26]. The performance differences among annealed samples and over time are still much. Therefore, annealing does not work much if any.



Fig 4.3 Plots of annealing tests

4.1.2 Light emission characteristics of p6P LETs

For light emission, the work is concerned about testing repeatability of results and optimizing the parameters for measurement before optimizing p6P LETs. The applied voltage (Vg) is a 100 kHz sinusoidal wave. Light emission intensity from each sample is measured three rounds with three different amplitudes of Vg-100V, 150V and 180V. Please note that the font difference is to distinguish from the amplitude of periodical signal-Vg). In another word, Vg=Vg*sin (wt+ φ). As shown in Fig 4.4, the repeatability of a sample is quite good. Between the first two rounds, the difference is within 10%. It means the sample does not degrade significantly during operation.



Fig 4.4 Intensity plot of triple measurements

Moreover, in order to locate a proper driving frequency for p6P LETs, the relationship between light emission intensity and driving frequency is also investigated. The result is plotted in Fig 4.5. The intensity is almost linear to driving frequency. The measured dependence fits well to linearity as shown in Fig 4.5. Higher frequency means more cycles of hole-electron recombination over time. The driving frequency for testing SAM treatment fixed at 100 kHz.



Fig 4.5 Plot of intensity dependence on driving frequency and linear fitting plot, R^2 is relevance coefficient between fitting line and the measured data.

In summary, the attempts to extract standard specifications and stabilize samples did not succeed due to low yield and performance variances over time and between samples. Annealing did not improve the stability over time. The light emission measurement is repeatable.

In order to get reliable results during SAM optimizing verification, principles for characterization are developed as below.

1. All samples receive identical I-V measurements.

2. The same kind of measurement for all samples is done almost the same time to all samples (differences within a few hours).

The settings for I-V measurement are simplified as Vg=0, Vds sweeping from 0 to 60V. For light emission, the driving voltage (Vg) is 100 kHz sinusoidal wave.

4.2.1 I-V characteristic improvement

I-V measurements are achieved from 3 reference samples, 6 OM treated samples and 4 PFDT

treated samples. The average currents of each group are plotted in Fig 4.6. The results from each sample are plotted in Appendix-5. The average values of Ids are compared when Vds is equal to 60V. The average current of the untreated group is below 4e-12A. All samples treated with the OM SAM except the first one have currents around 3e-11A. The PFDT SAM treated samples' currents are above 1e-10A. In average, PFDT treated samples are approximately 30 times better than untreated samples, and OM treated samples are over 10 times better.



Fig 4.6 Average I-V plots of three groups

Both SAMs improves contact resistance. The results are not expected if only work function modification is considered. PFDT is to decrease HIB, but OM is to increase HIB.

In the literature[18], the work function difference of gold $\Delta\Phi$ is 0.6ev after the application of PFDT. $\Delta\Phi$ is -0.8 ev after coating hexadecanethiol (CH3-(CH2)15-SH). OM only has two more CH2 than hexadecanethiol. Therefore, the $\Delta\Phi$ caused by coating OM shall be around -0.8 ev.

The work function modification theory alone is not effective to explain the results, since the two SAMs change work function of gold in the opposite way. A SAM introduces more factors contributing to decreasing contact resistance. The factors can be i) interfacial tunneling through the SAM, ii) SAM-induced modifications of interface morphology, and iii) the interface

electronic structure, iv) the active layer thickness that dominates the interface contact resistance [6].



Fig 4.7 Energy diagram for illustration of HIB modification

4.2.2 EL improvement

In the project, to describe light emission mechanism, the model is the same as that employed in [16]. As seen in Fig 4.5, drain and source electrodes are grounded and gate voltage is AC-biased. Such configuration is unconventional. Usually, there is a biased voltage between the drain and source electrode. Strictly speaking, under this configuration, the device is not a three-end device any more. Even if the drain or source is not grounded, light emission is still seen from the grounded electrods (drain or source).

Under this configuration, holes and electrons are periodically injected into p6P close to the interface. During the first half period, when Vg is above a threshold value, holes are injected into p6P from metal. The injected holes recombine with electrons, which are injected during a previous half period. EL is periodically induced. As shown in Fig 4.6, light emission is observed exclusively along the electrode edges.



Fig 4.8 Illustration of light emission-1. Equivalent circuit 2. Gate voltage plot (its value is relative) 3.Hole injection 4. Injected electrons recombine with holes



Fig 4.9 EL image with adjusted contrast--dotted line is a scratch on the sample surface

Light emission is measured from 2 untreated and 3 OM coated and 5 PFDT coated samples. The average intensity from three groups in relation to the amplitude of Vg is plotted in Fig 4.5. The intensity at Vg=87.5 V is used for comparisons. The light intensity from PFDT treated group is about 3.5 times higher than that from untreated group. The OM treated group is 2 times better.



Fig 4.10 Average intensity of three groups under AC driving, drain/source grounded

4.3 SAM characterization

The diameter of light source used by the ellipsometer is oversized, compared to the small feature size of the FET substrates. Therefore, two big chips (3mm long*5mm wide) are prepared for the thickness measurement of a SAM. The two chips have the same layer stack as depicted in Fig 3.10, but have different monolayers. Each sample is measured at three different points on its surface. In Table 4.1, it is the results from ellipsometry measurements. The average thickness of the OM SAM is 6nm, and the error range is over 2.8nm. The average thickness of PFDT-SAM is 1.3nm, the error rang is over 2.5nm. Meanwhile, the thickness of Au is fitted. For the OM coated chip, the thickness is 45.5nm, error range over 1.5nm. For PFDT-coated one, the thickness is 42.7nm, error range over 1.2nm. Both goodnesses of fit are over 0.976.

OSAM	thickn	ess(nm)	Au thickn	ess(nm)	goodness	\mathbf{of}	fit
	5.8092	+ -2.7582	45.5644	+ -1.5036		0.9	825
	6.0786	+ -2.6568	45, 4249	+ -1.4278		0.9	9767
	6.258	+ -3.2211	45, 5927	+ -1.7469		0.9	9767
PSAM	thickn	ess(nm)	Au thickn	ess(nm)	goodness	of	fit
PSAM	thickn 1.0478	ess(nm) + -2.4983	Au thickn 42.5751	ess(nm) + -1.1806	goodness	of 0.9	fit 9825
PSAM	thickn 1.0478 1.4173	ess(nm) + -2.4983 + -2.7391	Au thickn 42.5751 42.9075	ess(nm) + -1.1806 + -1.3188	goodness	of 0.9 0.9	fit 9825 9798

Table 4.1 results from ellipsometry measurements on coated two chips

In the literature [23], the thickness of PFDT is 1.67nm, and the thickness of CH3-(CH2)9-SH (DT) 1.37nm. OM (CH3-(CH2)17-SH) is the same with DT but a longer tail. Its thickness shall be less than 2.74nm. Obviously, the results in Table 4.1 are not reliable. This can be due to the complexity of the layer stack. If the layer stack is simplified to Au on silicon substrate with a SAM, more accurate results shall be obtained. But from the results in Table 4.1, at least it demonstrates the existence of OM SAMs. And also, the PFDT SAM is thinner than the OM SAM.

Chapter 5 Conclusion and Outlook

The object of the project is to optimize p6P thin film FETs by SAMs. The following conclusions can be made based on results obtained in the project.

Conclusion 1: As discussed in Chapter 4, despite the different polarization of their dipoles, both molecules improve I-V characteristics. The channel conductance is improved over 30 times and 10 times better by the PFDT-SAM and the OM-SAM respectively under equivalent conditions (Vg=0, Vds sweeps to 60V).

Conclusion 2: The theory of metal work function modification theory alone is not sufficient to explain I-V characteristic improvement by a SAM on electrodes. The results obtained from the project can be taken as another evidence for the idea proposed in the literature [6].

Conclusion 3 : Light emission intensity is increased by both of the SAMs. For instance, when the gate driving voltage is 87.5V, 100kHz sinusoidal with amplitude, PFDT-SAM treated samples give 3.5 times higher light emission intensity, OM-SAM treated ones 2 times.

Conclusion 4: The working principles of light emission from p6P FET (like other p-type LEFETs) are not well understood yet. Therefore, it is hard to explain how a SAM improves light emission. However, it is safe to say that charge injection is enhanced by the monolayer.

Conclusion 5: The performance of p6P FETs varies over time, which agrees with the observation in the literature[26].

Conclusion 6: Photoconductivity of p6P is significant. With illumination, current can be over four times higher.

In short, the optimizations of p6P thin film FETs by SAMs are significant on I-V characteristics and light emission intensity. The working principles of SAMs on electrodes, p6P FETs' stability

and photoconductivity are open to investigations.

The project can be developed further in the following aspects.

First, identify more SAM-introduced factors contributing to performance enhancement. A convenient approach can be to observe time-resolved light emission intensity from p6P LETs in response to driving voltage. By comparing SAM-treated samples with a reference group, holes or electron injection enhancement might be observed. Decay time differences of EL intensity might be acquired as the work done with tetracene FETs by Yuki Ohshima[28]. The time-resolved signal may offer more insights into working mechanisms of p6P FETs and SAMs.

Second, optimize the fabrication of p6P FETs. The yield shall be increased and the performance of p6P FET has much room to be improved. A simple-to-implement approach is to coat a thin transparent layer on p6P FETs. By this method, the p6P is isolated from moisture and impurities from the ambient environment.

Third, test if a SAM optimizes p6P nanofiber LETs. It can be expected that a SAM on electrodes improves nanofiber FETs, too. The challenge from the fabrication part is to transfer p6P fibers from the mica substrate. Currently, the fibers are transferred manually by rolling on a FET substrate as depicted in Fig 5.1. The mica with fibers is taped on a cylinder. Before transferring fibers, the FET substrate are wetted by vapor[27]. When the cylinder with mica is rolling over, the fibers are adsorbed to the FET substrate because of capillary action between condensed water and fibers. The problem is that the p6P fibers are very fragile. If the cylinder is pressed too much to the substrate while rolling, the structure of the fibers can be easily damaged. Moreover, after transferring, the alignment of nanofibers is lost. In short, the success of optimizing nanofiber transistors by SAMs highly relies on the mastering of transfer technology.



Fig 5.1 Transferring fibers from mica to FET substrate by rolling-on



Fig 5.2 Fluorescent images of transferring failures, (left) the part over gaps are missing and (right) alignment of fibers is lost.

To conclude, the application of a SAM significantly improves opto/electric performances of p6P LETs and there is still much to explore about p6P LETs and SAMs from the fabrication aspect to working principles.

Appendix

Appendix-1-FET Substrate Recipe

Back-gate Fabrication:

- 1. **Starting wafer:** Si (1 0 0), 4", single-side polished, 525μ m, high n-doped, $0.001 0.006\Omega$ ·cm, with 300nm SiO₂.
- Spin on photo resist: EBS11 spinner, thickness = 1.5μm, (0 RPM for 4 sec to deposit photo resist;
 500 RPM for 5 sec, 4000 RPM for 30 sec), prebake at 90°C for 60 sec, resist: AZ 5214E.
- Back gate exposure: KS mask aligner, exposure time = 2 sec, soft contact, inversion bake at 130°C for 100 sec, flood exposure for 25 sec.
- 4. Develop: AZ 351B, 22.0°C, 60 sec, rinse in water --2 min. spin dry
- 5. Check
- 6. Etch out back gate windows in oxide: bHF 7min (etch rate ~75nm/min, and this rate is not reliable; it's better to check by eye whether the SiO2-blue color is completely gone after HF etch; if not, HF etch should repeat with a reasonable extra time), rinse in water -- 5 min.
- Deposit Ti/Au: Cryofox 600 thin film deposition system, e-beam evaporator, thickness = 2/48nm, rate = 0.2Å /sec for Ti/Au.
- 8. Lift off Ti/Au: Acetone sonic agitation ~10 min, rinse in water -- 2min, spin dry.
- 9. Check

Drain/Source Electrodes Fabrication:

- Spin on photo resist: EBS11 spinner, thickness = 1.5μm, (0 RPM for 4 sec to deposit photo resist;
 500 RPM for 5 sec, 4000 RPM for 30 sec), prebake at 90°C for 60 sec, resist: AZ 5214E.
- Electrodes exposure: KS mask aligner, exposure time = 2.0 sec, soft contact, inversion bake at 130°C for 100 sec, flood exposure for 25 sec.
- 3. **Develop:** AZ 351B, 22.0°C, 60 sec, rinse in water --2 min. spin dry.
- Deposit Ti/Au: Cryofox 600 thin film deposition system, e-beam evaporator, thickness = 2/48nm, rate = 0.2Å /sec for Ti/Au.
- 5. Lift off Ti/Au: Acetone sonic agitation ~10 min, rinse in water -- 2min, spin dry.
- 6. **Check**

Coat photoresist before dicing

1. **Spin on photo resist:** EBS11 spinner, thickness = 1.5μ m, (0 RPM for 4 sec to deposit photo resist; 500 RPM for 5 sec, 4000 RPM for 30 sec), prebake at 90°C for 60 sec, resist: AZ 5214E.

Appendix-2- p6P Thin Film Deposition Manual

a. put sample in transfer chamber

- 1. the vacuum valve in the center closed
- 2. the 2 valve at right open
- 3. the valve at left open
- 4. sample plate in transfer chamber

b. put sample in deposition chamber

- 5. the 2 valve at right closed
- 6. the valve at left closed
- 7. the vacuum valve in the center open
- 8. after the pressure of transfer chamber is around 1e-2 mbar, turn on power supply for turbo pump connected to transfer chamber
- 9. two valves at right open
- 10. wait ~20 min
- 11. compressed air open
- 12. plug in the compressed air (the two chambers are connected)
- 13. put the sample in deposition chamber
- 14. unplug the compressed air

C. deposit p6P thin film

- 15. the oven power supply DC=1.15 A. Note the oven supply and time
- 16. increase the oven power supply to DC=2.2 A. Note the oven supply and time again
- 17. Wait until there is a rate. Note the base pressure (typical value around 1e-8mbar)
- Turn on the thickness monitor and press start/stop. Open the shutter. Restart the thickness monitor. Note the rate (around 0.1Å/s)
- 19. Wait thickness you want. Note the oven temperature and deposition pressure.
- 20. close shutter. Turn off the oven.

D. get sample out

- 21. open compressed air
- 22. take sample out of the deposition chamber
- 23. disconnect and close compressed air
- 24. close the valve at the center
- 25. turn off power supply for the turbo pump connected to transfer chamber.

- 26. Wait 20 min
- 27. Open the valve at left
- 28. Take sample plate out of the transfer chamber

E. resume the system

- 29. Close the transfer chamber
- 30. Close the valve at left
- 31. Close the 2 valve at right
- 32. Open the valve at left
- 33. after the pressure of transfer chamber is around 1e-2 mbar, turn on power supply for turbo pump connected to transfer chamber
- 34. two valves at right open

Appendix-3- User Interface of LabVIEW Program

for I-V measurement



Appendix-4- User Interface of LabVIEW Program for Light Intensity measurement





Appendix-5-I-V measurements on three groups









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