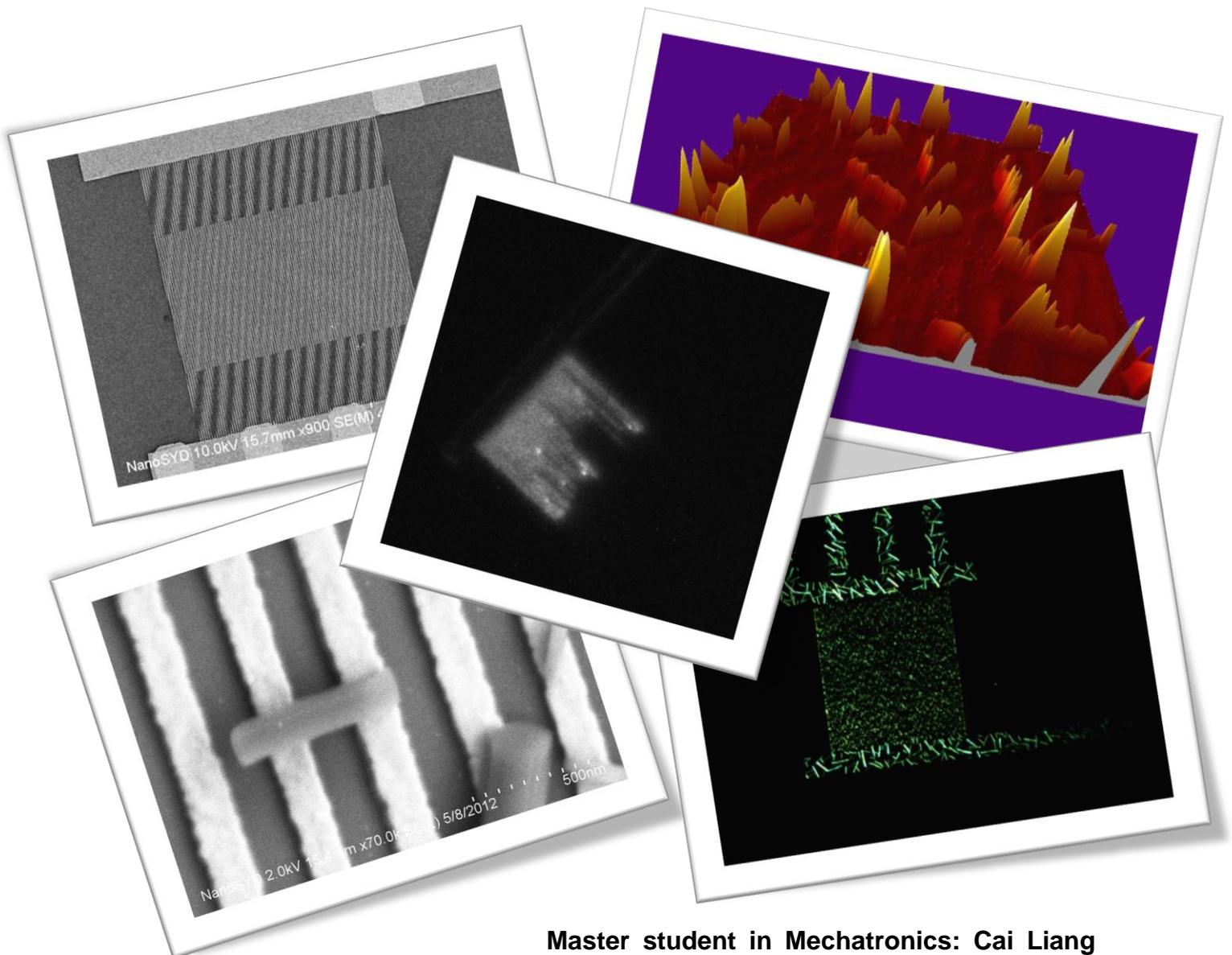


Nano OLETs: Nanoscale Organic Light-Emitting Transistors



Master student in Mechatronics: Cai Liang

Supervisor: Jakob Kjelstrup-Hansen

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Front cover images:

Upper left: SEM image of fabricated electrodes by e-beam lithography

Upper right: AFM 3D image of PPTTPP nanofibers on a gold substrate

Center: Optical micrograph of light emission from an OFET

Down left: SEM image of PPTTPP nanofiber deposited on electrodes

Down right: Fluorescence microscope image of PPTTPP nanofibers on electrode

Preface

This master thesis describes the outcome of my theory studies and practical experiments on OLETs (organic light emitting transistors) in NanoSYD, Mads Clausen Institute at University of Southern Denmark. My supervisor is Jakob Kjelstrup-Hansen. This project started in September of 2011 and continued until June of 2012. It has an extent of 40 ECTS.

During my final project, many people have offered their helps, which I really appreciate. First, I would like to thank my supervisor Jakob Kjelstrup-Hansen, who not only introduced the whole process to me, but also helped me to fix out various issues during the project, theoretically and experimentally. Then, many post docs and PHD students also offered great helps to me, such as Xuhai Liu gave me good advice of operating SEM and also helped me design the electrodes for EBL, Per Baunegaard With Jensen provided the matlab programs to deal with the light emission images and showed me how to operate the PPTTPP chamber and how to do the wire bonding for the light emission experiment, Roana Melina de Oliveira Hansen gave me great suggestions on how to deal with the PMMA residuals on the substrates and showed me how to operate the oxygen plasma etcher, Luciana Tavares gave me many suggestions and guidance about operating the probe station to test the prepared transistor samples, and Jacek Fiutowski also gave me some advice of operating SEM. Moreover, I also need to thank Kasper Thilsing-Hansen, the technical manager, who taught me how to operate AFM and change the tip for AFM, Moreover, he showed me how to charge the wire bonder's needle.

Abstract

5,5'-di-4-biphenyl-2,2'-bithiophene (PPTTPP) is an organic molecule that can be applied to OLET technology for research. In this project, the main aim is to fabricate and characterize PPTTPP nanofibers and investigate the photoelectric properties of PPTTPP material.

For PPTTPP nanofibers growth, the first hand of data about the size of PPTTPP nanofibers growing on a gold surface has been measured and recorded by AFM. The nanofibers have also been investigated by fluorescence microscope and SEM. After several deposition tests, I found the suitable process conditions to grow the nanofiber long enough to cross electrodes on the chip.

In the micro-fabrications, I firstly fabricated the electrodes connections on the transistor substrates by photolithography, metal deposition and dicing processes. For fabricating the connections, I developed a new process recipe, which can save one time of metal deposition and lift-off compare to the previous recipe. Two types of silicon wafers have been used to in this project, N3 and N4 with SiO₂ thicknesses of 100nm and 200nm, respectively.

Then, by using e-beam lithography and metal deposition, nano scale electrodes on the substrates were formed. During this process, I tested out the best dosefactors for e-beam lithography. To optimize the result, I tried to use the oxygen plasma etch after the development to remove the residual PMMA on the surface. After several tests, I found the best etch time and etch power, so that the electrodes are formed perfectly. Since the process period to fabricate a chip of transistor is quite long, I also discovered a novel method to reuse the chips which have already deposited PPTTPP nanofibers. With this new method, it can not only save the experiment time, but also save the experiment cost.

After that, through the electrical tests, the good samples without current leakage or short circuits were selected out to do the PPTTPP deposition under the optimized process conditions. During tests, I discovered N3 type of wafer with 100nm thick SiO₂ might not suitable to fabricate the transistor substrate, as the current leakage through the gate dielectric layer was too high when a relatively high gate voltage was applied.

Finally, light emitting experiments on PPTTPP nanofibers OLETs have been carried out. Based on these experiments, photoelectrical properties of PPTTPP have been studied. Moreover, the transistors were quite easy to destroy once high voltage or frequency was applied. However, in order to make the nanofibers emitting light, high voltage or high frequency are required, because of the injecting barrier between the nanofibers and

electrodes. So the future work is to reduce the injecting barrier, improve the emitting efficiency of the transistors, and extend the lifetime of transistor.

Keywords: PPTTPP, Organic Light Emitting Transistor, Nanofibers, In-Situ Growth, AC Gated Ambipolar OLEFETs

Glossary

AC: Alternating-Current

AFM: Atomic force microscopy

BC/BG: Bottom Contact/Bottom Gate

BC/TG: Bottom Contact/Top Gate

EBL: Electron-Beam Lithography

FETs: Field-Effect Transistors

FWHM: Full width at half maximum

HOMO: Highest occupied molecule orbital

IPA: 2-propanol

LUMO: Lowest unoccupied molecule orbital

OLED: Organic Light Emitting Diodes

OLEFETs: Organic Light-Emitting Field-Effect Transistors

OMBD: Organic molecular beam deposition

PMMA: Poly(methyl methacrylate)

p6P: para-hexaphenylene

PPTTPP: 5,5'-di-4-biphenyl-2,2'-bithiophene

TC/BG: Top Contact/Bottom Gate

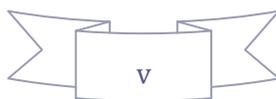


Table of Contents

Preface.....	ii
Abstract.....	iii
Glossary	v
Table of Contents	vi
Chapter 1: Introduction	1
Chapter 2: Nanofibers.....	3
2.1 Molecules	3
2.1.1 p6P (Para-hexaphenylene) Molecules.....	3
2.1.2 PPTTPP (5,5' -di-4-biphenyl-2,2' -bithiophene) Molecules.....	4
2.2 Nanofiber Growth and Investigation.....	4
2.2.1 Nucleation Process and Growth Modes	5
2.2.2 p6P Nanofibers Growth on Mica.....	7
2.2.3 PPTTPP Nanofibers Growth on Flat Gold.....	9
2.2.4 Characteristics of PPTTPP Nanofibers on Flat Gold	10
Chapter 3: Devices: Organic Field-Effect Transistors.....	13
3.1 Basics of OFETs.....	13
3.2 Device Structures.....	14
3.3 Working Principle of OFETs.....	15
3.3.1 Operating regimes of OFETs.....	16
3.3.2 Current-voltage Relationship.....	17
3.3.3 Energy Level Analysis.....	18
3.4 Unipolar and Ambipolar OFETs.....	20
3.4.1 Unipolar OFETs	20
3.4.2 Ambipolar OFETs	21
3.5 Organic Light-Emitting Field-Effect Transistors	22
3.5.1 Direct-Current (DC) Gated Ambipolar OLEFETs.....	23
3.5.2 Alternating-Current (AC) Gated Ambipolar OLEFETs	25

Chapter 4: Fabrication of Organic Light-Emitting Field-Effect Transistors	27
4.1 Photolithography.....	27
4.2 Electron-Beam Lithography (EBL).....	29
4.2.1 Dosefactor Test	30
4.2.2 Issues and Solution in EBL	36
4.3 PPTTPP Nanofibers Growth on Structure Devices	39
4.4 How to Remove PPTTPP Nanofibers from Transistor Substrates	40
Chapter 5 Light Emission Experiment.....	42
5.1 Experimental	42
5.2 Results and Discussion.....	44
5.2.1 Gate Voltage Dependent Light Emission.....	44
5.2.2 Frequency Dependent Light Emission.....	47
5.2.3 Damaged Samples	50
Chapter 6 Conclusion and Outlook.....	51
Appendix A: Recipe for p6P deposition.....	54
Appendix B: Recipe for PPTTPP deposition	62
Appendix C: Former Photolithograph Recipe of Transistor Substrate	66
Appendix D: Improved Photolithograph Recipe of Transistor Substrate	70
Appendix E: Recipe of Dicing	75
Appendix F: Step by Step Procedure of EBL.....	78
Appendix G: Program to Measure the light intensity in Voltage Sweeping Test.....	80
Appendix H: Program to Measure the light intensity in Frequency Sweeping Test	84
Appendix I: Short Circuit Test for Fabricated Electrodes of Transistors	88
Reference	91

Chapter 1: Introduction

Nanotechnology has increasingly affected our daily life. Generally, the scale ranges from 1 to 100 nanometres and there are two methods to fabricate the devices or structures into this nanoscale: Top-down technology and Bottom-up technology¹. Quantum mechanical effects are important at this quantum-realm scale.²

The applications of nanotechnology can cover many areas in our lives, and one of the applications is light emitting devices. For instance, inorganic semiconducting crystalline nanowires made from III-V materials have been investigated to fabricate nanowire field-effect transistors³, multicolor light sources⁴, lasers⁵, photo detectors⁶ and solar cells⁷ based on their well-defined properties.

Recently high performance electric and optoelectronic devices based on organic semiconductors have also been demonstrated, such as organic light emitting diodes (OLED)^{8,9}, field-effect transistors (FETs)¹⁰, and solar cells¹¹. These organic devices show promise for low-cost, large-area and flexible devices. In particular, display panels using OLED are expected for mobile electronic devices and excellent stability and high efficiency OLED have been reported. On the other hand, rapid progress of organic light-emitting field-effect transistors (OLEFETs) has been made in recent years.¹²

OLEDs usually are integrated in another class of organic light-emitting devices, which require transistors controlling their luminance. By comparison, in OLEFETs, the luminance can be adjusted by changing only the gate voltages, instead of applying any additional devices. Therefore, OLEFETs show a great advantage of largely decreasing both the number of devices and the circuit complexity.

Although OLEFETs research is still at the early stage, plenty of exciting results have been demonstrated. The first OLEFET based on a Tetracene Thin Film has been reported in 2003.¹³ Then, P-type, N-type and even ambipolar OLEFETs have been developed in succession.^{14,15} In addition, Alternating-Current (AC) gate voltages has been applied to operate the OLEFET in 2008.¹⁶

Nowadays, para-hexaphenylene(p6P) as the light-emitting organic semiconductor has been studied a lot in OLEFETs in the NanoSYD group. It can self-assemble into crystalline nanofiber structures that emit polarized, blue light up on UV excitation.^{17,18} Whereas, a new material 5,5'-di-4-biphenyl-2,2'-bithiophene (PPTTPP) has rarely been investigated for applying on the transistors. The properties of PPTTPP still need to be investigated.

So the main object of this project is to fabricate and characterize PPTTPP nanofibers on a gold planar surface and determine PPTTPP nanofibers optimum growing condition,

under which PPTTPP nanofibers are long enough to cross the electrodes. Then it is to fabricate a transistor substrate and grow nanofibers on the gold electrodes with the optimized growth conditions. Finally, it is to characterize the electrical and optical properties of PPTTPP nanofibers on the fabricated substrates.

In chapter 2, two kinds of organic materials, which have been used in OLETs, are introduced first. Then the principle of nanofiber growth is explained. Finally, PPTTPP nanofibers have been fabricated and characterized by AFM, SEM and fluorescence microscope. First hand data of the size of nanofibers have been recorded.

In chapter3, the working platform, organic field-effect transistors are presented, including the structure, classification, and working principle. In chapter 4, the process of fabricating the devices is introduced in detail.

The optical properties of PPTTPP have been recorded in chapter 5 by light emitting experiment.

Finally, in chapter6, the conclusion of the project has been summarized. Moreover, the future work and investigation are discussed in the last chapter.



Fig.1.1.1: the possible application of OLETs: flexible and colorful display

Chapter 2: Nanofibers

In this chapter, two different active organic materials applied in this project are going to be introduced. Then, the nucleation process and growth modes of organic nanofibers will be briefly explained and the experimental data including the optimized process conditions for growing long nanofibers will be presented. With the nanofibers are characterized by AFM (atomic force microscopy), the statistical experimental data and calculation of nanofibers are presented.

2.1 Molecules

The two kinds of nanofibers made by p6P and PPTTPP molecular are organic fluorescence materials, as mentioned in Chapter1. p6P is a promising material for the electroactive layer in organic colored LED displays, because of its blue luminescence with high quantum yield¹⁹. Recently, PPTTPP, based on its good properties²⁰, is also increasingly attracting researchers' interest.

2.1.1 p6P (Para-hexaphenylene) Molecules

Para-hexaphenylene(p6P), $C_{36}H_{26}$, is chain of six phenyl rings, as shown in fig.2.1.1.

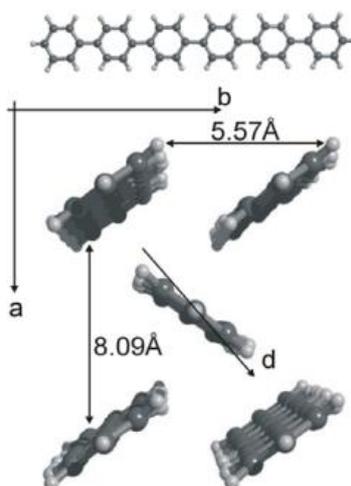


Fig.2.1.1: p6P molecule and crystal structure with crystal lattice constants. (Adopted from²⁰)

In the carbon ring, the orbital of carbon atoms form the σ bonds with each other. Meanwhile, the orbital which is perpendicular to the molecular plane, bonding with the neighboring molecule, forms the π bonds. Since π bonds are much weaker than σ bonds, the valence electrons are delocalized. That is why the conductivity of crystalline p6P is found to be highly anisotropic, with a preferred conduction perpendicular to the long molecular axes.²¹ Moreover, the charge density in the center

part of molecule is higher than the two ends, so the electrical conduction mainly focuses on the center part of two neighboring molecules.²² As for the optical properties, the luminescence and the optical absorption of crystalline p6P are polarized along the long axis of the molecules.

These molecules can be evaporated in ultra-high vacuum from a Knudsen cell. By depositing p6P on different substrates, the molecules can be either lying or standing upright on the substrate surface, and can form either continuous films or p6P nanofibers, depending of the substrate chemical and physical properties and also the growing conditions, such as temperature and thickness of deposition.

2.1.2 PPTTPP (5,5'-di-4-biphenyl-2,2'-bithiophene) Molecules

PPTTPP molecules are similar with p6P molecules, as they just use bithiophene to replace biphenyl in the centre of the molecule chain, as shown in fig.2.1.2. According to this, the two molecules have many similar properties.

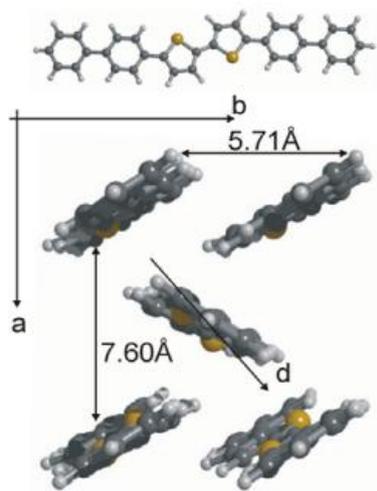


Fig.2.1.2: PPTTPP molecule and crystal structure with crystal lattice constants.
(Adopted from²⁰)

PPTTPP can also self-assemble into microscopic crystalline aggregates or nanofibers by the organic molecular beam deposition in vacuum chamber. Similar to p6P, charge transport in PPTTPP crystal occurs via incoherent hopping between the neighboring molecules through the intermolecular π bonds. Comparing to p6P charge mobility, which is around $0.3\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, the largest charge mobility of PPTTPP can reach to $1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$.²⁰ Besides, PPTTPP crystal nanofibers can also emit polarized and highly anisotropic photoluminescence output under UV light. And the emission color is green due to the different electronic transition energy between the highest occupied molecule orbital (HOMO) and the lowest unoccupied molecule orbital (LUMO).

2.2 Nanofiber Growth and Investigation

In this section, first the nucleation process and growth modes of organic crystals will be introduced. Then p6P nanofibers deposited on a mica substrate are going to be investigated. Initially, so I deposited p6P on mica for practice, even all the parameters for p6P have already been studied before. Afterwards, I started the PPTTPP deposition on 50 nm thick gold thin film on silicon substrate and tried to find the suitable growing conditions for the PPTTPP nanofibers being long enough to cross the gap between the FET electrodes (the gap between the electrodes is around 200nm). Finally, the PPTTPP nanofibers have been characterized by AFM, and all the data have been recorded and analyzed.

2.2.1 Nucleation Process and Growth Modes

As p6P and PPTTPP oligomers are hardly dissolvable, all the molecules have been deposited by vacuum sublimation from the Knudsen cell. The deposition rate ranges usually from $0.05\sim 0.2\text{\AA s}^{-1}$, which is measured by a quartz microbalance. The base pressure of the vacuum system is typically from $5\times 10^{-7}\text{mbar}$ to $1\times 10^{-8}\text{mbar}$, and the thickness of deposition ranges from 5nm to 6nm. (For more details please see the deposition recipes in the appendix A and B.) Such organic molecular beam deposition (OMBD) is a good method to get the high quality and clean crystalline aggregates under vacuum condition, as it is an easy way to control the super-saturation and the final thickness of the deposited material, with at the same time an independent control of the substrate temperature.

As we know, crystallization process is a phase transition process, which means the mobile phases change into the solid phase of crystal. In our situation, the vapor of the materials is deposited on the solid substrate, which usually goes through four steps: collision, absorption, nucleation and nanofiber or thin film growth.

Once the gas molecules impact on the substrate surface, either elastic scattering or inelastic scattering will happen first. For elastic scattering, there is not energy exchanged, but momentum transferred. So it is kind like a specular scattering, and molecules usually return back to gas phase. As for inelastic scattering, when molecules loss enough energy, they are trapped to the surface, and transfer into a bound adsorbate state.

According to absorption, it can be divided into two types: physical absorption and chemical absorption. The first one refers to the absorption without any electron transfer between the adsorbate and the substrate. And the adsorbate is attracted by van der Waals forces. This type of adsorption is very typical for most of the organic molecules impinging on a substrate surface. Compare to this one, chemical absorption relates to the electron transfer between the adsorbate and the substrate, which means the chemical bond forms. This case usually happens when the inorganic materials deposit

the substrate. And it often occurs after the physical absorption and dissociation process. Generally speaking, the chemical absorption is stronger than the physical absorption, so the organic molecules are much weaker bound on the substrate comparing to inorganic materials forming compounds. These two processes have been shown in fig.2.2.1.

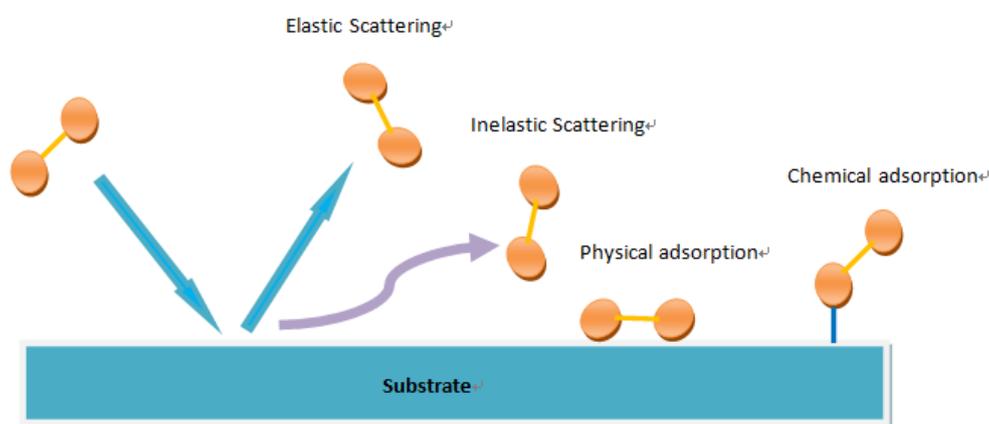


Fig.2.2.1: collision and adsorption processes illustration

As deposition continues, the concentration of the molecules in the vapor is increasing. Accordingly, an increasing number of molecules have been adsorbed on the surface. In accordance with the nucleation and growth mechanism, small clusters of molecules, or so called nuclei, are formed first. Generally speaking, nucleation is the spontaneous formation of small embryonic clusters with a critical size determined by the equilibrium between their vapor pressure and the environment pressure. The formation of nuclei is in a metastable supersaturated or undercooled medium. And nucleation is a precursor of the crystallization process. If by any chance the critical radius of the clusters increases slightly, then the clusters will continue to grow until a macroscopic two-phase equilibrium is achieved. Otherwise, the clusters will disappear or evaporate again. Fig.2.2.2 shows the relation between the vapor pressure of cluster and their size.

After the nucleation forms, based on the interactions with substrate and between molecules, nanofibers or thin film growth can be divided into three basic modes: islands growth (Volmer-Weber growth), layer growth (Frank-van der Merwe growth) and island-layer growth (Stranski-Krastanov growth). They are illustrated in fig.2.2.3. If the growth species more strongly bound to each other than to the substrate, islands will generate until they coalesce to form a continuous film. This growth mode we call islands growth or Volmer-Weber growth. For example, many metal deposit on ceramic or semiconductor substrates growing in this mode. If the growth species bind more strongly to the substrate than to each other, first a complete monolayer will form, before the deposition of the second layer. This growth mode is called layer growth or

Frank-van der Merwe growth. This growth mode often occurs when single crystal films epitaxial grow on substrates.

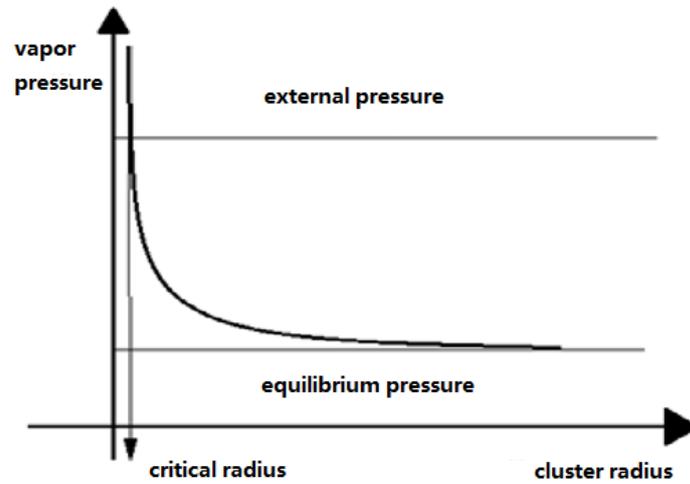


Fig.2.2.2 vapor pressure of clusters according to their size (adopted from²³)

Between these two modes, there is a transition mode, island-layer growth (Stranski-Krastanov growth) mode, which is layer growth followed by island growth. It typically involves stress, which is developed during the formation of the nuclei or films. In our case, for instance, p6P nanofibers grow on mica, which grows in this mode. More details will follow in next section.

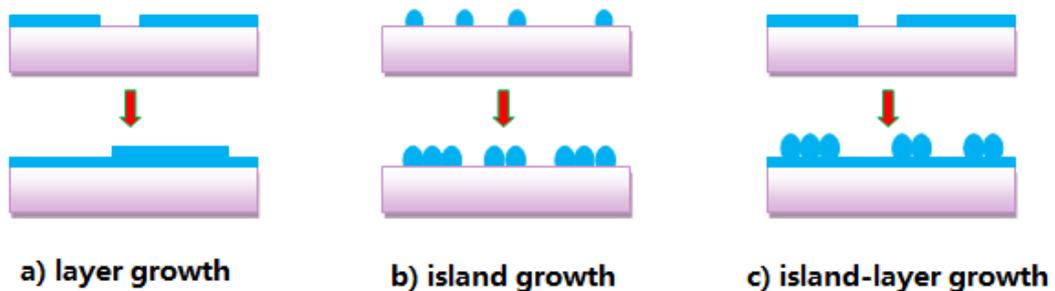


Fig.2.2.3 three basic nucleation and growth modes of crystallization

Overall, small clusters of molecules, so-called nuclei, are formed first, which further agglomerate to form islands. As growth proceeds, agglomeration increases, chains of islands or nanofibers are formed and eventually join up to produce a continuous deposit, which still can contain channels and holes. These holes eventually fill up to give a continuous and complete film and further growth leads to smoothing of the surface irregularities or in contrary these defects can be enhanced by further overgrowth.

2.2.2 p6P Nanofibers Growth on Mica

Muscovite mica was chosen as substrate due to the extremely smooth surface of mica can offer relative homogeneous plane for nanofibers growth. The deposited nanofibers

are crystalline, dimensions largely depend on growth conditions and typical ranges are from a few tenths of μm to mm in length, up to tenths of nm in height and up to a few hundred nm in width.

As mentioned before, in p6P molecules, hydrogens around the molecule can be regarded as being positively charged due to the relative high electronegativity of carbon atoms in the inner part of the molecule. Consequently, coulomb interaction occurs between neighboring p6P molecules, leading to a so called herring-bone structure in the p6P crystal, where all long molecular axes are parallel, see fig.2.2.4. And the lattice constants are shown before in fig.2.1.1. Due to this edge-to-face alignment, the π -orbital overlaps among neighboring molecules can be improved, resulting in relative high electrical conduction in crystal. Moreover, the mutual orientation of the molecules gives rise to a very pronounced polarization of the fluorescence, which is a useful feature for investigating the crystallinity of a sample.²⁴ This is obviously showed in fig.2.2.5 (a) and (b), which are taken under polarized filter.

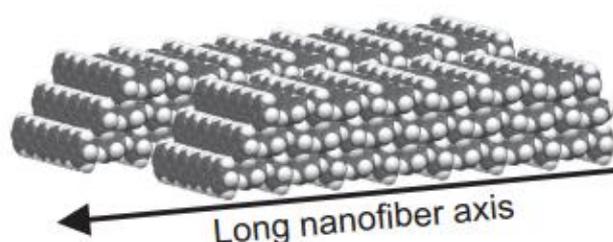


Fig.2.2.4: structure of p6P crystalline nanofiber with long nanofiber axis indicated

According to the layer-island growth mode we discussed in the last section, when p6P deposit on the mica surface, the molecules first form a wetting layer of lying molecules, growing with their (111) and (211) faces parallel to the substrate and self-assembling, then grow into nanofibers. And the growth direction of the nanofibers is according to one of the muscovite high symmetry directions. That is because the mica surface has relatively high interaction with p6P molecules due to the dipole field on the freshly cleaved mica surface.²⁵ It is illustrated in fig.2.2.5. The images of p6P nanofibers growing on mica are taken by fluorescence microscope. It is not difficult to find that all the nanofibers are growing in certain direction.

Furthermore, the nanofiber growth can also be affected by growth conditions, such as deposition rate, base pressure and thickness of deposited materials. One of the most important growth conditions is the substrate temperature. Two groups of deposition under different temperatures are shown in fig.2.2.5 (c) and (d). It is obvious that the nanofibers are shorter and denser for lower temperatures, and grow longer when the temperature is increased. This is because of the diffusion coefficient of the molecules,

which is increased when the substrate temperature increase, leading to the result molecules can diffuse a long distance to form the longer fibers.

But once the temperature is higher than a certain temperature, when molecules are not easy to stick to the substrate, the nanofibers become shorter again and even evaporate into gas phase again (this will be illustrated by the images in next section).

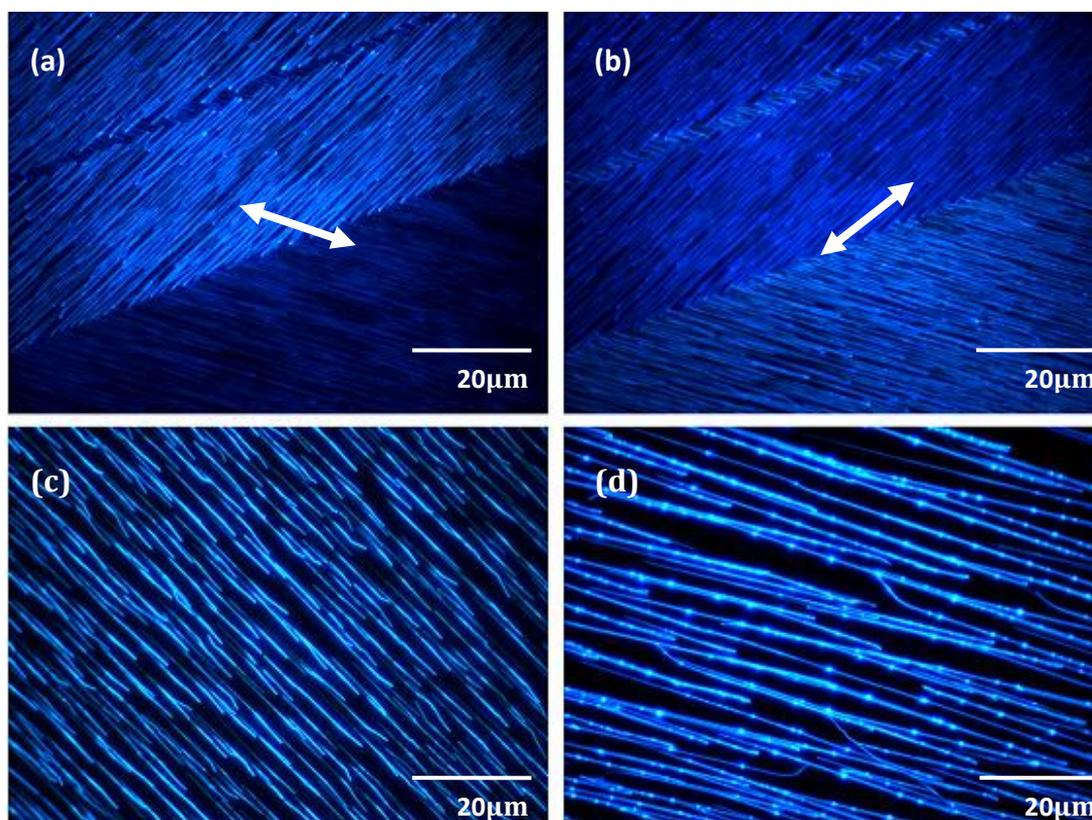


Fig.2.2.5: fluorescence images of p6P nanofibers grown on mica. (a) and (b) are taken under polarized filter with filter rotating 90° between each measurement. Polarizer directions are indicated by white arrows, which indicates the luminescence output from p6P nanofibers is aligned perpendicular to the long nanofibers axis; (c) and (d) are under different substrate temperature, 473K and 480K, individually.

2.2.3 PPTTP Nanofibers Growth on Flat Gold

Nanofibers growing on mica are long, straight and mutually parallel. However, mica is fragile and not processable. Moreover, mica is not a thermal or electric conducting material. So if we want to apply the nanofibers to the optoelectronic devices, transfer technology is essential. The other possible approach is in-situ growth, which means to grow the nanofibers directly on the electrodes made of for example a thin gold layer. Therefore, I made the deposition tests of PPTTP on planar gold. The gold surface was prepared by depositing 10nm titanium and 50nm gold on a silicon substrate.

As we know, the surface energy is very important for the resulting nanofibers morphology, since it influences the molecular arrangement in the nanofibers. The

surface energy of freshly cleaved mica in vacuum is around 5000 mJ m^{-2} while it is around 1400 mJ m^{-2} for gold²⁶²⁷. So the interaction between nanofibers and gold is not as strong as the one between nanofibers and mica. Compare to the long and oriented nanofibers grown on mica, nanofibers grown on gold are short and random. And their growing temperatures are different, as PPTTPP nanofibers growing on mica at around 508K while growing on gold at around 423K (the other conditions are the same, base pressure at around 10^{-7} mbar ,deposition rate 0.1 \AA/s and deposited thickness $5\sim 6\text{nm}$, more details please check appendix B).

In order to find the suitable temperature for PPTTPP nanofibers growing longer on gold surface, three groups of tests have been carried out, and the results are showed in fig.2.2.6.

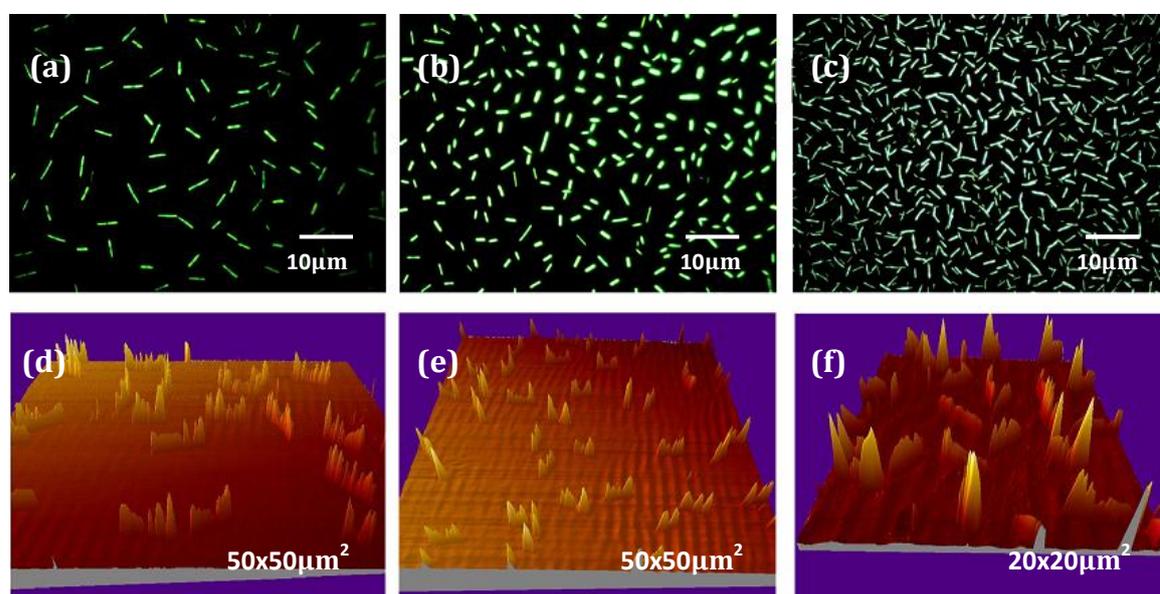


Fig.2.2.6: Fluorescence images and AFM 3D images of PPTTPP nanofibers deposited on 50nm thick gold surface. Nanofibers in (a) and (d) are deposited under 423K and 2.8×10^{-7} mbar, the deposited thickness is 5.2nm; nanofibers in (b) and (e) are under 433K and 1.3×10^{-7} mbar, the thickness is 5.4nm; for these in (c) and (f) are under 443K and 1.2×10^{-7} mbar, the thickness is 5.6nm.

According to fluorescence images, nanofibers grown under 423K seems to be relative longer. In order to confirm this point, AFM measurements have been taken.

2.2.4 Characteristics of PPTTPP Nanofibers on Flat Gold

Nanofibers measurements have been taken in three samples, with different deposition temperatures: 423K, 433K and 443K. Since nanofibers in the same sample can grow in various sizes, so in order to make the measurements more close to true value, each sample has been taken the measurements three times in different area. Samples have first been scanned by AFM. For 423K and 433K sample, the density of nanofibers is

relative low, so the scan size is $50 \times 50 \mu\text{m}^2$, which including around 30 nanofibers. Whereas, the density of 443K sample is high, so the scan size is reduced to $20 \times 20 \mu\text{m}^2$, which also including about 30 nanofibers. Then the images are analyzed by SPIP software, including length, height and full width at half maximum (FWHM) measurements.

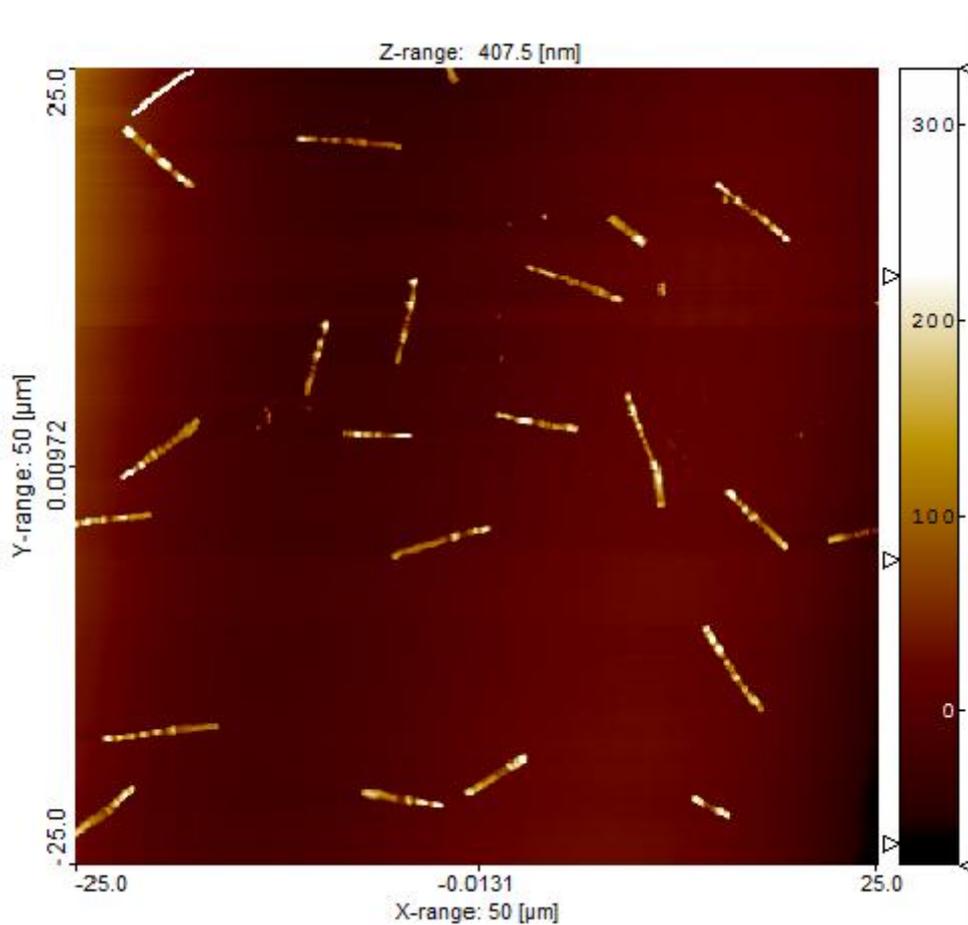
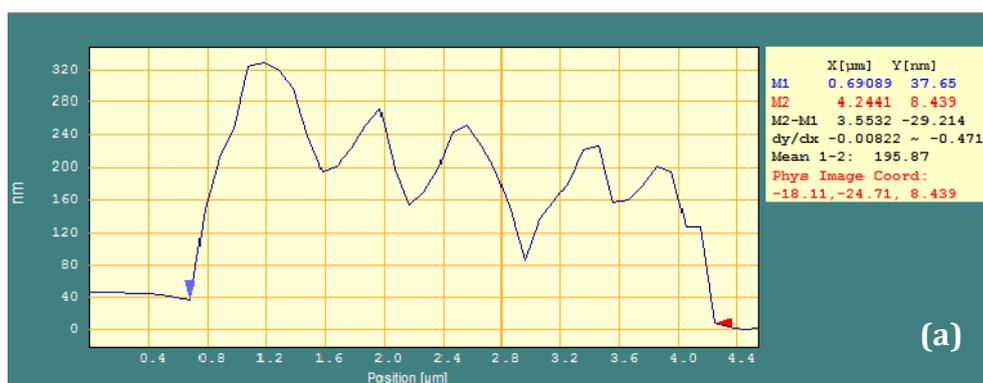


Fig.2.2.7: AFM image of measuring 423K nanofibers



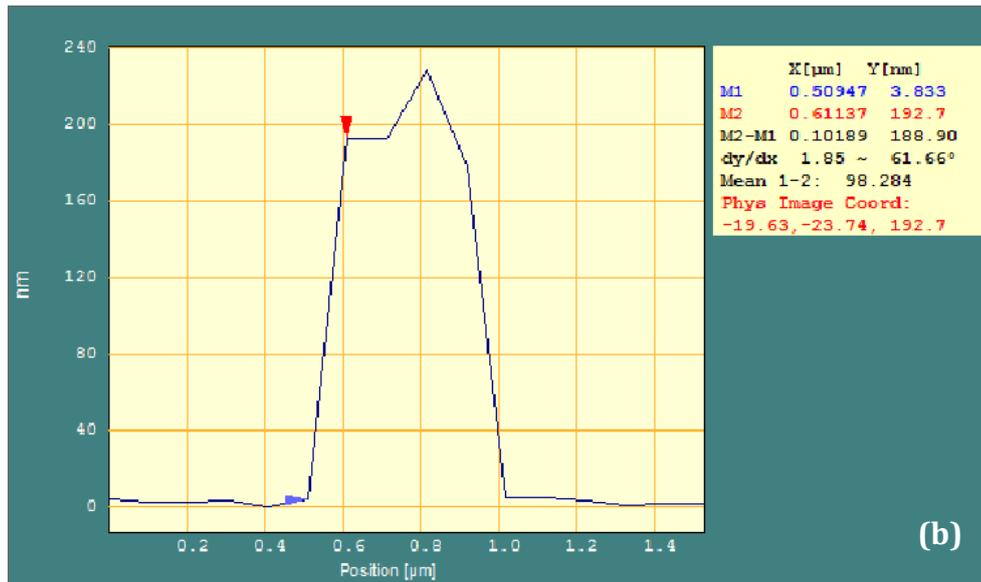


Fig.2.2.8: SPIP measurement of 423K nanofiber's (a) length and height; (b) FWHM

Based on these data, the average values and standard deviations of the length, height and FWHM have been calculated out (Table 2.1).

Table 2.1: Data of the sizes of PPTTPP nanofibers under different growth temperature

Samples with different deposition temperatures	Average Length \pm S.D.(μm)	Average FWHM \pm S.D.(μm)	Average Height \pm S.D. (nm)
423K	5.70 \pm 1.4	0.49 \pm 0.11	0.14 \pm 0.02
433K	4.32 \pm 1.65	0.49 \pm 0.12	0.16 \pm 0.03
443K	3.10 \pm 0.82	0.31 \pm 0.10	0.10 \pm 0.02

According to the table 2.1, it is obvious that the average length of 423K nanofibers is the longest. So the growth temperature for the later deposition on transistor substrates is determined at 423K.

Chapter 3: Devices: Organic Field-Effect Transistors

In this chapter, OFETs, the working platform of nanofiber devices, will be described in detail. The basics of OFETs will be introduced firstly. Then, three types of common field effect transistor configurations are presented with their advantages and disadvantages. Next, the working principle of OFETs is explained. Then, the charge carriers transport channels are classified. Finally, OLEFETs, including direct current (DC) gated OLEFETs and alternative current (AC) gated OLEFETs are presented.

3.1 Basics of OFETs

An organic field-effect transistor (OFET) is a field effect transistor using an organic semiconductor in its channel. Organic crystalline materials can be either in-situ grown by vacuum evaporation or transferred of a peeled single-crystalline organic layer onto a substrate. Field effect transistors as a powerful tool can be used to investigate organic semiconductors, such as charge transport and light emission properties.

Moreover, these devices can be developed to realize low-cost, large-area, and flexible electronic products, and even biodegradable electronics. So they are increasingly attracting researchers' interests.

Generally speaking, an OFET consist of three components²⁸: an organic semiconductor (thin film or nanofibers), a dielectric layer and three electrodes (drain, source and gate). They can be divided into two parts. One part works as a conducting channel between two ohmic contacts, which are called the source and the drain contacts. The other part works to control the charge induced into the channel, and it is called the gate. The direction of the movement of the carriers in the channel is from the source to the drain. Hence the relationship between these three components is that the gate controls the carrier movement from the source to the drain.

Organic semiconductor materials can be highly ordered molecular crystals such as tetracene, pentacene and rubrene.²⁸ As for gate electrode, it can be metal or conducting polymer. But usually, highly doped silicon is chosen to be the gate and substrate as well. Because the substrate is silicon, the gate dielectric layer usually is made of thermally grown silicon oxide. Besides, it can also be Al_2O_3 and Si_3N_4 or organic insulators, for instance, poly (methyl methacrylate) (PMMA)¹⁵ depending on the transistor structure. The source and drain electrodes which contact with semiconductors, are usually made of metals, such as gold, silver²⁹ or calcium¹⁵. Printable conducting polymers, such as PANI³⁰ can be the other choice for electrodes.

In this project, the semiconductors are in-situ growth p6P or PPTTPP nanofibers. Highly doped silicon works as the gate electrode and the substrate, with 100nm or 200nm

silicon oxide being the gate dielectric. Source and drain consist of 10nm Ti and 50nm Au. More details are shown in chapter 4 about how to prepare the device.

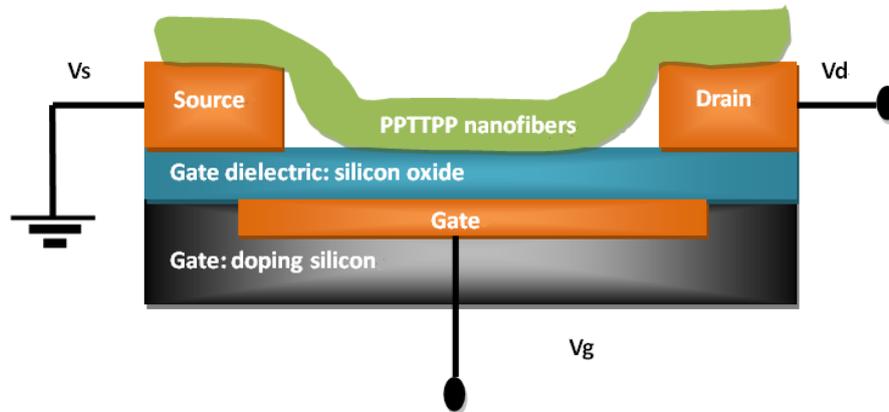


Fig.3.1.1: Schematic structure of a field-effect transistor

For device operation, a voltage is usually applied on the drain electrode (V_d) and gate electrode (V_g), while the source electrode is grounded ($V_s=0v$). The charges (holes or electrons) are injected from the source electrode.

3.2 Device Structures

According to the position of the contacts and gate to the semiconductor, OFETs can divide into three basic configurations: Bottom Contact/Bottom Gate (BC/BG), Top Contact/Bottom Gate (TC/BG), and Bottom Contact/Top Gate (BC/TG) configurations. They are shown in fig. 3.2.1.

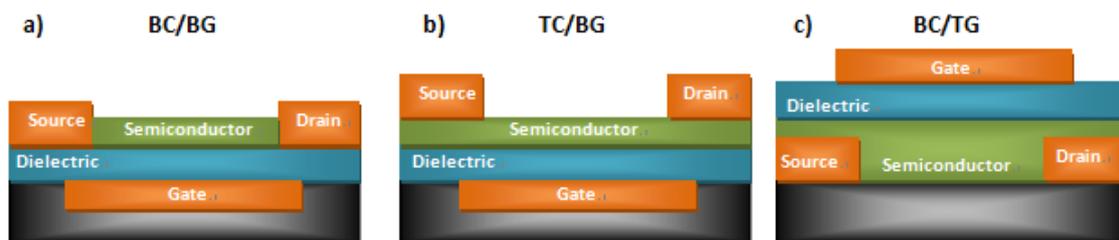


Fig.3.2.1: Three OFETs configurations: a) Bottom Contact/Bottom Gate (BC/BG); b) Top Contact/Bottom Gate (TC/BG); c) Bottom Contact/Top Gate (BC/TG)

In BC/BG structure, doped silicon layer usually serves as back gate. Then dielectric layer can be silicon oxide growing on the top of silicon substrate. Source and drain electrodes can be fabricated by photolithography and metal deposition processes. Finally, organic semiconductor is deposited on the device. The obvious advantage for this structure is it is easy to be fabricated. And it is also high efficiency because of photolithograph process. But the interface between the semiconductor and electrodes

are limited to the sidewall of the electrodes, so it will have high injection resistance for the charge carrier injecting into the semiconductor. In this project, OFET devices are fabricated in this structure.

As for TC/BC structure, since the source and drain electrodes are on the top of semiconductor layer, the semiconductor should be deposited first. Consequently, the electrodes cannot be fabricated by photolithography, as the organic layer would be damaged by the photolithography process. Usually, stencil technology is applied to fabricate the electrodes instead. It showed in fig.3.2.2. So the process is more complicated and less efficient. And the metal deposition can also cause certain damage to contact area between electrodes and organic layer. On the other side, because the contact interface between the electrodes and organic layer is the bottom area of electrodes, which is much larger than the area of electrodes sidewall, the injecting resistance is decreased.³¹

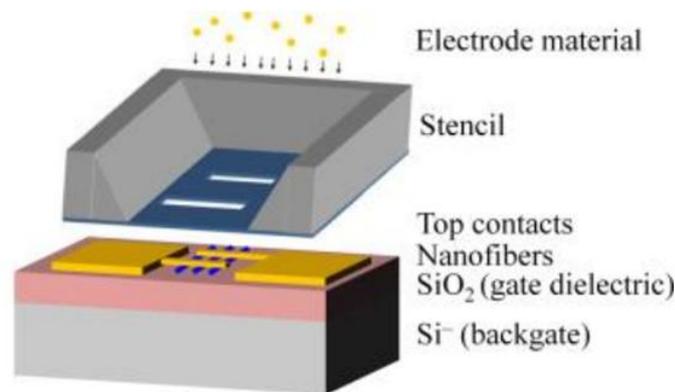


Fig.3.2.2: Illustration of stencil technology to form the top contact electrodes

Compare to these two structures, BC/TG structure can avoid these issues mentioned before. The interface is increased as the charge carrier can not only be injected from the sidewalls of electrodes, but also from the parts of electrodes that overlap with the gate electrode. Moreover, source and drain electrodes are fabricated before the organic layer deposition, so they can be formed by photolithography with high efficiency and the damage to the organic layer by the metal deposition is also avoided. The only issue is SiO_2 cannot be grown on the substrate as dielectric layer, as it has to form after the semiconductor deposition. Instead, an organic dielectric layer is applied by spin-coating process.³²

3.3 Working Principle of OFETs

In order to simplify the analysis, we assume the OFETs are the BC/BG structure, as what I used in this project. And the source and drain electrodes are the rectangle shape, with

width of W , and they are separated by the distance of L , as shown in fig.3.3.1. Since nanofibers are grown randomly between the electrodes, which is difficult to analyze the current passing through the channel, we assume a semiconductor layer growing between source and drain electrodes.

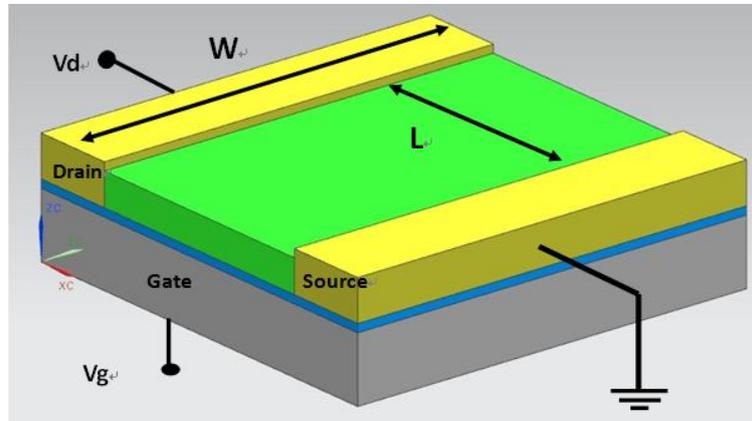


Fig.3.3.1: Schematic structure of OFET with channel length L and channel width W

3.3.1 Operating regimes of OFETs

As we know, the transistor actually works as a capacitor when the gate voltage is applied. So the positive charge carriers (for P type channel) are accumulated at the interface between semiconductor and dielectric layer when negative V_g is applied. Likewise, the negative charge carriers (for N type channel) are accumulated when positive V_g is applied. These charge carriers can induce the current from source to drain. According to the capacitance definition, the accumulate charges is proportional to V_g and the capacitance of dielectric layer. However, not all the charges can be mobile to form the current, as the charges first have to fill traps at the interface. After the traps are filled, the additional charges are able to move and induce the current. That is why there is a threshold voltage V_t . And the effective gate voltage should be $V_g - V_t$.

When no V_d is applied or $V_d \ll V_g - V_t$, the charge density in the channel is almost homogeneous, or there is a linear gradient of charge density from source to drain. This is a linear regime, as the current I_d through channel is proportional to V_d (shown in fig.3.3.2 a). And the potential $V(x)$ within the channel increases linearly from 0 at source ($x=0, V(x)=0$) to V_d at drain ($x=L, V(x)=V_d$).

As V_d increased to the value $V_d = V_g - V_t$, the channel is “pinched off”, which means a depletion regime forms close to drain electrode (shown in fig.3.3.2 b). This is because the potential difference between local potential $V(x)$ and gate voltage V_g starts to be smaller than threshold voltage V_t . So there are not accumulated charges or only trapped charges at that regime. A space-charge-limited saturation current $I_{d,sat}$ can flow across this depletion area as carriers are swept from the pinch-off point to the drain by the

comparatively high electric field in the depletion region. Further increasing V_d , I_d would not increase as it reaches to the saturated value. But the depletion region becomes larger (shown in fig.3.3.2 c).

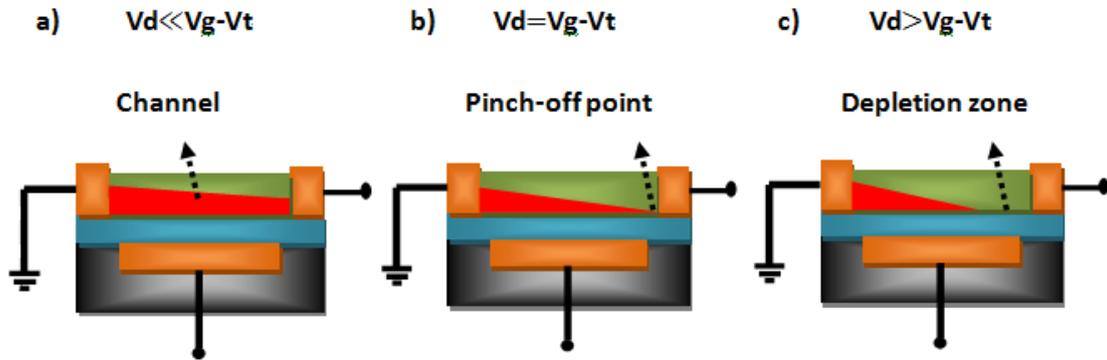


Fig. 3.3.2: illustrations of operating regimes of OFETs: a) linear regime; b) turn to be saturation regime at pinch-off point; c) saturation regime.

3.3.2 Current-voltage Relationship

Based on the calculation about the relationship between the current (I_d) and voltage (V_d and V_g), we can have a better understanding.

Since dielectric layer works as a capacitor, so the mobile charges per unit area Q_s are related to the local potential within the channel:

$$Q_s = C * (V_g - V_t - V(x)) \quad (\text{Equation 3.1})$$

where C is the capacitance per unit area of the dielectric layer. The charges in channel are supposed to occupy a rectangle bulk with height H . The length and width are equal to the channel's length L and width W (as shown in fig. 3.3.1).

According to Ohm's law, current density J is related to conductivity σ and electrical field E :

$$J = \sigma * E = Q_v * \mu * E = \frac{Q_s}{H} * \mu * E \quad (\text{Equation 3.2})$$

Where Q_v is the mobile charges per unit volume, μ is the charge mobility. Based on equation 3.2, the current from source to drain I_d can be determined by the following equation:

$$I_d = J * W * H = Q_s * W * \mu * E \quad (\text{Equation 3.3})$$

As electrical field E is related to the position, we can get $E = dV/dx$. Then input equation 3.1 into 3.3, the following equation is obtained:

$$I_d * dx = W * \mu * C * (V_g - V_t - V(x)) dV \quad (\text{Equation 3.4})$$

By integrate equation 3.4, with x from x=0 to x=L, according to V(x)=0 to V(x)=V_d, finally we get:

$$I_d = \frac{W}{L} \cdot \mu \cdot C \left[(V_g - V_t)V_d - \frac{1}{2}V_d^2 \right] \quad (\text{Equation 3.5})$$

When $V_d \ll V_g - V_t$, equation 3.5 can be simplified to:

$$I_d = \frac{W}{L} \cdot \mu_{lin} \cdot C \cdot (V_g - V_t)V_d \quad (\text{Equation 3.6})$$

From equation 3.6, we can see I_d is proportional to V_d , when V_g is a constant. That is why we called this regime linear regime.

Once $V_d \geq V_g - V_t$, equation 3.6 is no longer valid. As mentioned before, when $V_d = V_g - V_t$, I_d reached to saturation state, and it cannot increase anymore. Therefore, by replacing V_d with $V_g - V_t$ in equation 3.5, we can obtain the equation to calculate the saturation current in saturation regime:

$$I_{d,sat} = \frac{W}{2L} \cdot \mu_{sat} \cdot C \cdot (V_g - V_t)^2 \quad (\text{Equation 3.6})$$

Based on equation 3.6 and 3.7, we can get current-voltage characteristic curves, shown below (fig.3.3.3):

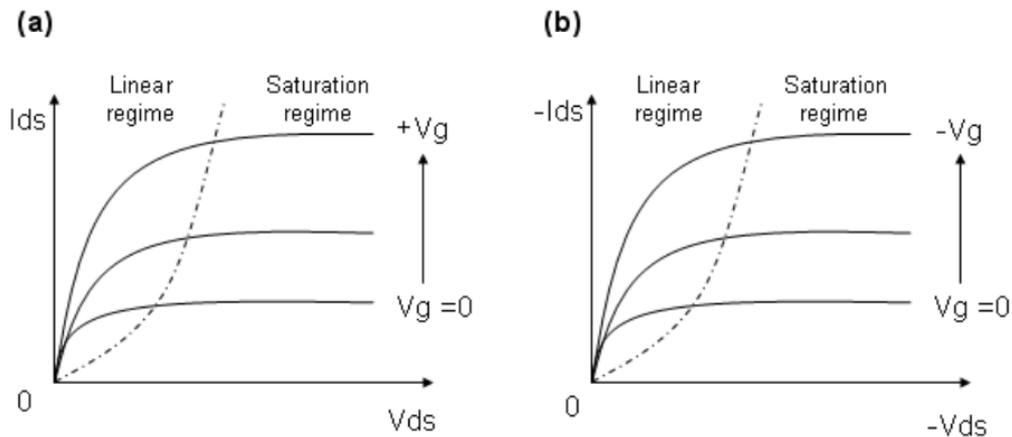


Fig.3.3.3: current -voltage output characteristics curves: a) for n-type semiconductors; b) for p-type semiconductors (adopted from²²)

In order for a field-effect transistor to reach saturation, short channel effects should be avoided by having a channel length that is at least 10 times larger than the gate oxide thickness.³³ However, in this project, the channel length is around 200nm, while the gate oxide thicknesses are either 100nm or 200nm, so the current cannot enter into saturation regime.

3.3.3 Energy Level Analysis

As for solid inorganic materials, the electrical properties are determined by band gaps or energy gaps. In the band structure of solid, the band gap generally refers to the energy difference between the top of the valence band and the bottom of the conduction band. This is equivalent to the energy required to free an outer shell electron from its orbit about the nucleus to become a mobile charge carrier, able to move freely within the solid material. So the band gap is a major factor determining the electrical conductivity of a solid. Since the energy gap of insulators is quite large, so they are not easy to form free electrons. As for conductors, the conduction band and valence band are overlapped, so little energy is required for conduction. While for semiconductors, certain energy is required for the electrons to jump into the conduction band.

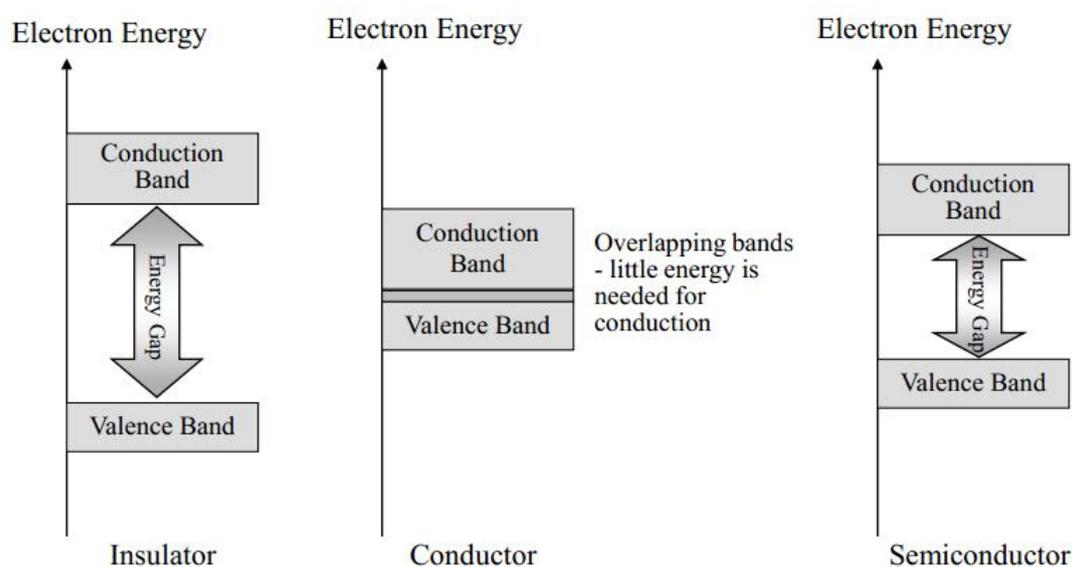


Fig.3.3.4: illustration of band gap for different types of solid materials

In contrast, HOMO (Highest occupied molecule orbital) and LUMO (Lowest unoccupied molecule orbital) are the corresponding concepts of valence band and conduction band to organic semiconductors. Moreover, in organic semiconductors, the current is formed by electrons jumping from one molecule to another (as mentioned in section 2.1.1), whereas in the inorganic semiconductors, the current is formed by delocalized electrons.

In our device, the source and drain electrodes are made of gold with relative high work function, whereas the organic semiconductor PPTTPP is in-situ grown on the top of electrons and bridging the gap between electrons. The HOMO and LUMO energy level of PPTTPP and the work function of gold are shown below (fig.3.3.5)¹⁵:

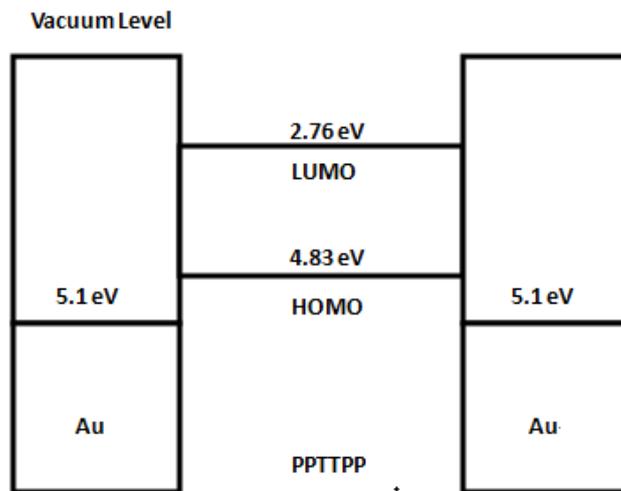


Fig.3.3.5: energy level of our device in the project when no voltage is applied

It should be noted that the HOMO and LUMO energy levels of the semiconductor can be affected by the gate. Specifically, applying a positive gate voltage "pulls" the energy level downwards. Oppositely a negative gate potential "pushes" the energy levels upwards.

In the other way, the electrodes energy level can also be affected by the applied voltage. By applying a positive drain voltage, the electrodes energy level is shifted down, whereas applying a negative drain voltage, the energy level is shifted up.

Generally, LUMO level approaches to the electrode energy level, electrons start to inject from electrodes into semiconductor, whereas the HOMO level is close to the electrode energy level, holes start to inject into semiconductor.

As for our device, the electrodes energy level is more close to HOMO level, so the semiconductor is more likely to work as a p-type semiconductor. If different electrodes with different work functions close to LUMO and HOMO level, respectively, the injection efficiency can be approved, and ambipolar operation becomes possible.¹⁵

3.4 Unipolar and Ambipolar OFETs

3.4.1 Unipolar OFETs

As for inorganic semiconductors, the distinction between p-type and n-type semiconductors is made entirely on the basis of extrinsic dopants being incorporated that are capable of inducing either holes in the valence band or electrons in the conduction band.

However, unlike the inorganic semiconductors, which need to be doped, organic semiconductors are used in high purity. That is because the small dopant in the organic

semiconductors can be mobile when the electrical field is applied.³⁴ And it is also difficult to directly observe the difference of transport properties of electrons and holes. So it is hard to determine the organic semiconductor to be p-type or n-type.

One method is to incorporate these intrinsic organic semiconductors into field-effect transistor configurations with a particular dielectric layer, so their charge transport characteristics can be evaluated. When applying negative gate voltages, many materials exhibit hole accumulation behavior. But when it turns to be positive gate voltages, less electrons are accumulated. For this kind of organic materials, in which only p-type channel is possible to form, we call them p-type organic semiconductors. Otherwise, if the material has high electron affinities, and only n-type channel seems possible to form in the material, we call it n-type organic semiconductor.

Accordingly, OFETs with p-type organic semiconductor applied are called p-channel OFETs, while OFETs incorporating with n-type organic semiconductor are called n-channel OFETs. Both p-channel OFETs and n-channel OFETs are called unipolar OFETs. Generally speaking, many organic materials behave like p-type organic semiconductors in OFETs, and many researchers are trying to synthesize and fabricate n-channel OFETs.

Recently, it has become clear that the chemical structure of the organic semiconductor is not the only factor that determines whether an organic FET exhibits predominantly p-channel or n-channel behavior. Processing and characterization conditions, device architecture, and choice of electrodes are important as well. The most important factor is the gate dielectric and charge trapping mechanisms the interface between dielectric layer and semiconductor.³⁵ So strictly speaking, it is not correct to speak of p-type or n-type semiconductors, instead with p-channel OFETs or n-channel OFETs.

3.4.2 Ambipolar OFETs

Further researches and experiments show that organic semiconductors are intrinsically ambipolar and thus capable of conducting both electrons and holes in suitable device configurations and under inert testing conditions. If an organic transistor can accumulate and transfer both electrons and holes in semiconductor depending on the applied voltages, we call it ambipolar OFETs.

Let us assume that the same positive voltages are applied on the gate and drain, i.e. $V_g=V_d$, and source is grounded. If the gate voltage is larger than the threshold voltage of electrons, i.e. $V_g > V_{t,e}$, electrons are injected from source and induced through semiconductor layer by the positive drain voltage. This is called unipolar regime.

While, if the gate voltage is decreased, and smaller than the threshold voltage of electrons, i.e. $V_g < V_{t,e}$, then no electrons are injected from source. Meanwhile, as the gate voltage decreased, it is negatively biased compare to drain voltage. If the value of

difference between gate and drain is larger than the absolute value of threshold voltage of holes, i.e. $V_d - V_g > |V_{t,h}|$ (threshold voltage of holes is a negative value), as for ambipolar transistor, holes will inject from the drain. However, for n-channel transistor, it would be in off-state.

In the medium situation, if $V_g > V_{t,e}$, and $V_d - V_g > |V_{t,h}|$, then both holes and electrons will be injected into the channel as for ambipolar transistors. And this regime is called ambipolar regime.

Recently, there are three main methods to fabricate ambipolar transistors, which contribute to three types of ambipolar OFETs: bilayer, blend, and single-component transistors²⁸ (Shown below in fig.3.4.1).

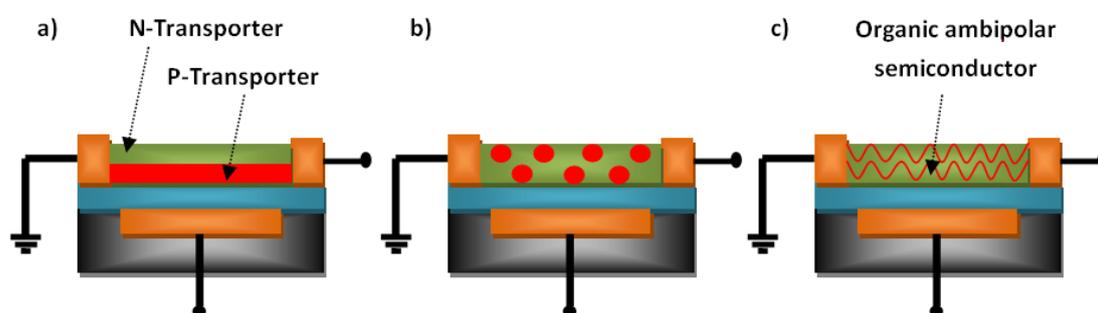


Fig.3.4.1: three types of ambipolar OFETs: a) bilayer; b) blend; c) single-component

However, in order to fabricate an ambipolar transistor, there are still many challenges need to fix out, such as efficient injecting both charges carriers, trapping charges carriers in semiconductor/dielectric interface. Moreover, how to keep the stability of charges transport under the ambient condition is another issue.

3.5 Organic Light-Emitting Field-Effect Transistors

One aim of semiconductor technology is to fabricate a device which can combine electrical functions (e.g. transistors) with optical functions (e.g. light source). Light emitting field effect transistors as one of special FETs can reach this aim pretty well, as it integrates the switching properties of transistors with the emission properties of light-emitting diodes (LEDs).

The first organic light-emitting transistor was reported in 2003 by Hepp et al.¹³ It based on Bottom Contact/Bottom Gate (BC/BG) structure, with tetracene thin films working as semiconductor layer. As it is unipolar (p-channel) OLEFET, so the light emission is very weak. And the emission only near to drain, which could be attributed to the difficulty of electrons to fully inject into organic semiconductor. Therefore, holes injected from the

source electrode have to move along the entire channel length to arrive at the drain electrode to recombine with much less electrons injected from drain.

Compare to the unipolar OLEFETs, ambipolar OLEFETs with holes and electrodes injected simultaneously, have high efficient recombination of charge carriers, leading to strong light emission. Usually, OLEFETs are operated by DC gate voltage. In 2008, Yamao et al. presented a new method by applying AC gate voltage, and the transistor with 300nm PPTPP thin films was lit up.¹⁶

In these transistors, the organic semiconductor is sandwiched between an anode and cathode with work functions suitable for injecting holes and electrons, respectively. The applied electric field drives holes at the energy level of the highest occupied molecular orbital (HOMO) while electrons are transported at the level of the lowest unoccupied molecular orbital (LUMO). When opposite charges meet they form an exciton which is localized on individual molecules. Due to the principle of conservation of energy, a part of excitons annihilate radioactively, while the rest give up their energy by heat. The relatively high resistance of intrinsic organic semiconductors leads to heating energy losses and the injection barriers are often significant. Both factors lead to high operating voltage, which is impractical as it will cause the electrodes melted. (This will be shown in chapter 6.) And low energy efficiency is also undesirable. All these issues are the main challenges in OLEFETs technology which still need to be fixed out.

3.5.1 Direct-Current (DC) Gated Ambipolar OLEFETs

As discussed in section 3.4.2, for ambipolar OFETs, there are two operating regimes: unipolar regime and ambipolar regime. Since the light emission only occurs when holes and electrodes recombine and emit the photons. So OLEFETs only work at ambipolar regime. The working principle of DC gated ambipolar OLEFETs is shown below:

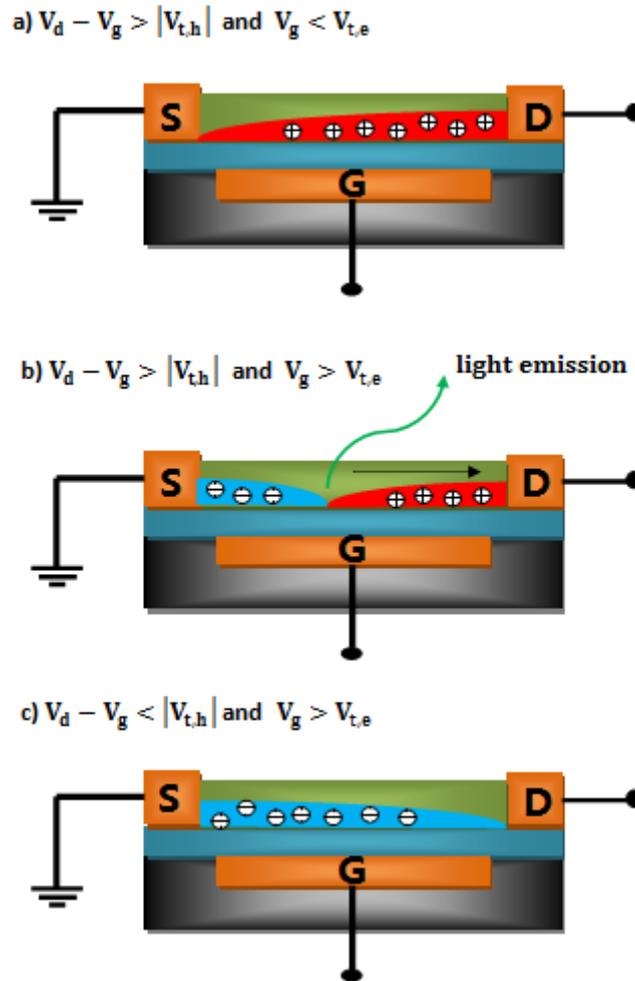


Fig.3.5.1: Illustration of operating a DC voltage gated ambipolar OLEFET

Similar to the process mentioned in section 3.4.2, when positive voltages are applied on the gate and drain electrodes, and drain voltage is more positive than gate, i.e. $V_d - V_g > |V_{t,h}|$ (as we know, $V_{t,h}$ is a negative value), holes will be injected from drain and accumulate in the channel. However, gate voltage is below the threshold voltage of electrons, i.e. $V_g < V_{t,e}$, so no electrons are injected from source. In this regime, there is no light emitting in the channel. This is shown in fig. 3.5.1 (a).

Next, when V_g is increased, $V_g > V_{t,e}$, the transistor enters into ambipolar regime, as electrons start to inject into the channel from source. Light emission takes place near the source electrode. By increasing the gate voltage, more electrons are injected into the channel, and fewer holes are accumulated in the channel. So the light emission line drifts from source to drain (shown in fig.3.5.1 (b)).

Then, when emission line arrives at drain electrode, namely $V_d - V_g < |V_{t,h}|$, no holes are injected and accumulate in the channel, and electrons occupy the whole channel. So the transistor enters into unipolar regime again and the light emission disappears (as illustrated in fig.3.5.1 (c)).

It is important to know that, the emission intensity stays constant while the emission line moves from one electrode to another, but it decreases when it moves near to electrodes. That is because of the influence from metal electrodes.

3.5.2 Alternating-Current (AC) Gated Ambipolar OLEFETs

According to Yamao' report,¹⁶ the operating electrical circuit of AC gated ambipolar OLEFETs is different from the circuit of DC gated ambipolar OLEFETs. The equivalent circuit is schematically shown in fig.3.5.2. Constant voltages are applied on the source V_s and drain V_d , while AC voltage with amplitude V_G and frequency f is applied on the gate electrode.

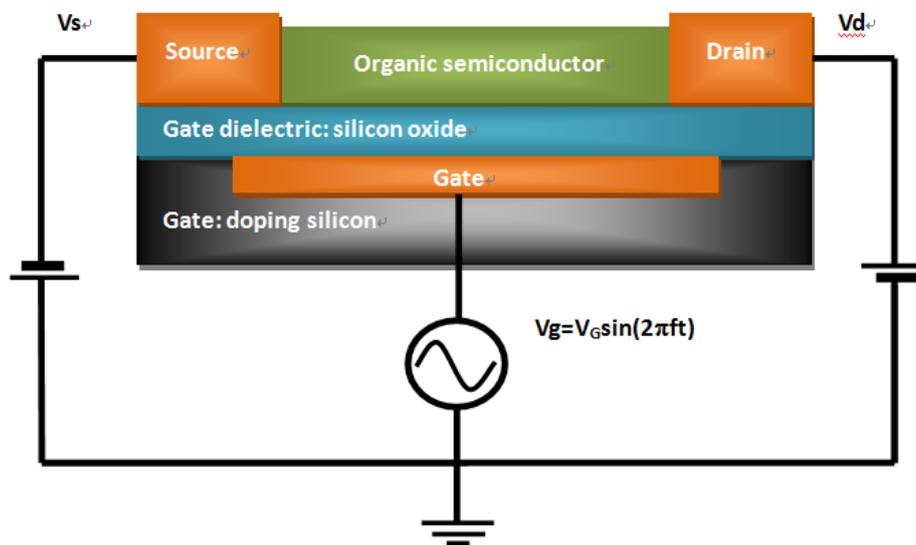


Fig.3.5.2: Schematic diagram of the electrical circuit that operates the AC gated ambipolar OLEFETs

The operation process is a bit similar to the DC gated ambipolar OLEFETs: assume the gate voltage starts from negative amplitude value, i.e. $V_g = -V_G < V_s$. As mentioned in section 3.3.1, at this stage, transistor enters into the saturation regime, so the channel is occupied by positive charge carriers. In next stage, gate voltage increase to the value of V_s , i.e. $V_g = V_s$, so it reaches the pinch-off point. The hole density near to the source electrodes is zero. As the gate voltage increase to positive value, electrodes start to inject into the channel from source electrode. When holes meet electrons, recombination takes place and light is emitted. However, the holes can also drift to the source electrodes by space-charge limited current flowing across the depletion area. That is why high frequency of gate voltage is needed, as electrons can be injected quickly enough, before the holes start drifting into the source. Moreover, applying high-frequency gate biases produces stronger light emissions.

Another method to operate AC gated OLEFETs is demonstrated by Xuhai L²². According to the report, the device can be lit up even with $V_d=V_s=0V$. And in this way, the light emission has nothing to do with the channel length if the frequency of gate voltage is high enough. Furthermore, even only one electrode (drain or source) connected to circuit, transistor still can emit the light, as the electrode can inject both holes and electrons.

When the AC voltage shifts to negative value, the electrical field will attract the holes out of the metal electrodes (no matter source or drain). The holes are accumulated in the semiconductor near the electrodes (shown in fig.3.5.3 (a)). Then, when the AC voltage transfers into positive value, the opposite electrical field forms and electrons are injected from the electrodes. If the frequency is high enough, the speed of shifting the AC voltage is so fast that the holes still stay in the semiconductor and meet the subsequently injected electrons, thus contributing to the light emission (shown in fig.3.5.3 (b)).

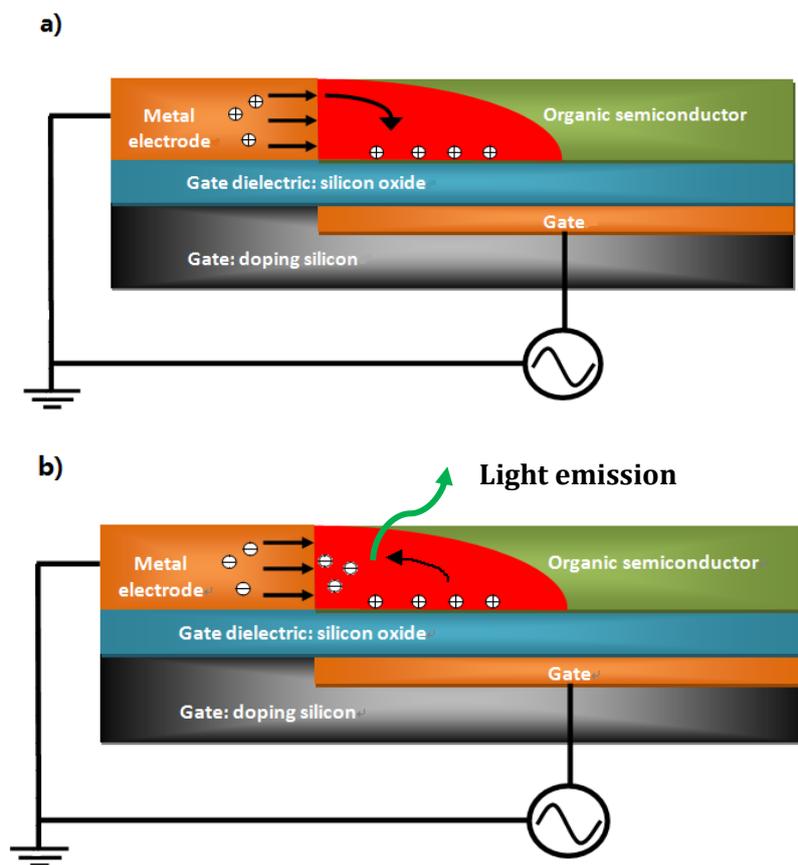


Fig.3.5.3: Illustration of operating principle for single metal electrode OLEFETs: a) the gate voltage shifts to negative value; b) the gate voltage shifts to positive value.

Chapter 4: Fabrication of Organic Light-Emitting Field-Effect Transistors

In this chapter, the experimental processes of how to fabricate the organic light emitting field effect transistors will be presented in detail, including photolithography, dicing, e-beam lithography, and metal deposition. For photolithography, a new recipe which can save one time of metal deposition and lift-off process has been invented. As for e-beam lithography, since the PMMA is out of date, the developing result is not good enough, so oxygen plasma etch is applied to remove the residual PMMA on the surface. Furthermore, as the time to fabricate the substrates is quite long, a novel method of reusing the deposited substrates has been invented, which can save lots of experiment time and cost.

4.1 Photolithography

Photolithograph process is highly efficient, as it uses ultraviolet light exposure to form the patterns on the photoresist, which has been spin-coated on the wafer surface. Because of the light diffraction, which will affect the final pattern printed on the resist, three types of photolithography have been invented to decrease diffraction effect - contact, proximity, and projection photolithography. In this project, contact photolithography has been used.

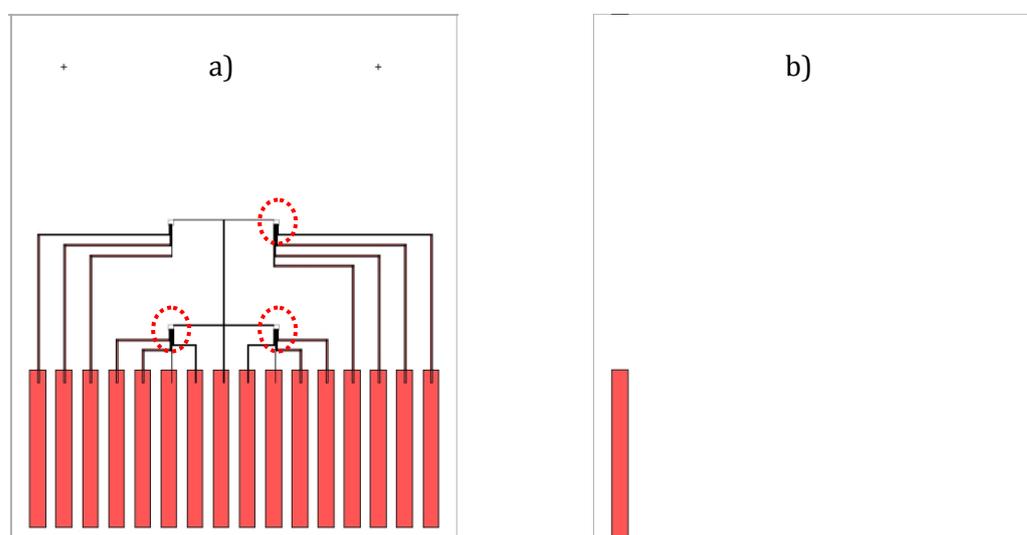


Fig.4.1.2: mask patterns for one chip; the size for one pattern is 10mm×8mm: a) one pattern from mask1 to fabricate the electrical connection to source and drain. The red dash line marks the areas used to do EBL and form the source and drain electrodes; b) one pattern from mask2 to fabricate the gate pad which has to contact with doped Si layer.

Patterned masks, usually composed of glass and chromium, are used during printing to cover areas of the photo resist layer that shouldn't get exposed to light. Development of

the photo resist in a developer solution after its exposure to light produces a resist pattern on the wafer, which defines which areas of the wafer are exposed for material deposition or removal. The structure of the transistor is Bottom Contact/Bottom Gate (BC/BG), as mentioned in section 3.2. There are two masks applied in this fabrication. One is used to form the electrical connection to source and drain on the surface of SiO₂ layer, the other is used to form the gate pad, which need to connect to the doped Si layer. (Masks patterns are shown in fig.4.1.2)

As a usual recipe, the electrical connections to source and drain are firstly formed by photolithography with mask1, followed with metal deposition. Then mask2 is used to form the etching mask for HF wet etching the SiO₂ layer, so that the holes are formed to doped Si layer. With the second metal deposition and lift-off process, the gate pads are formed.

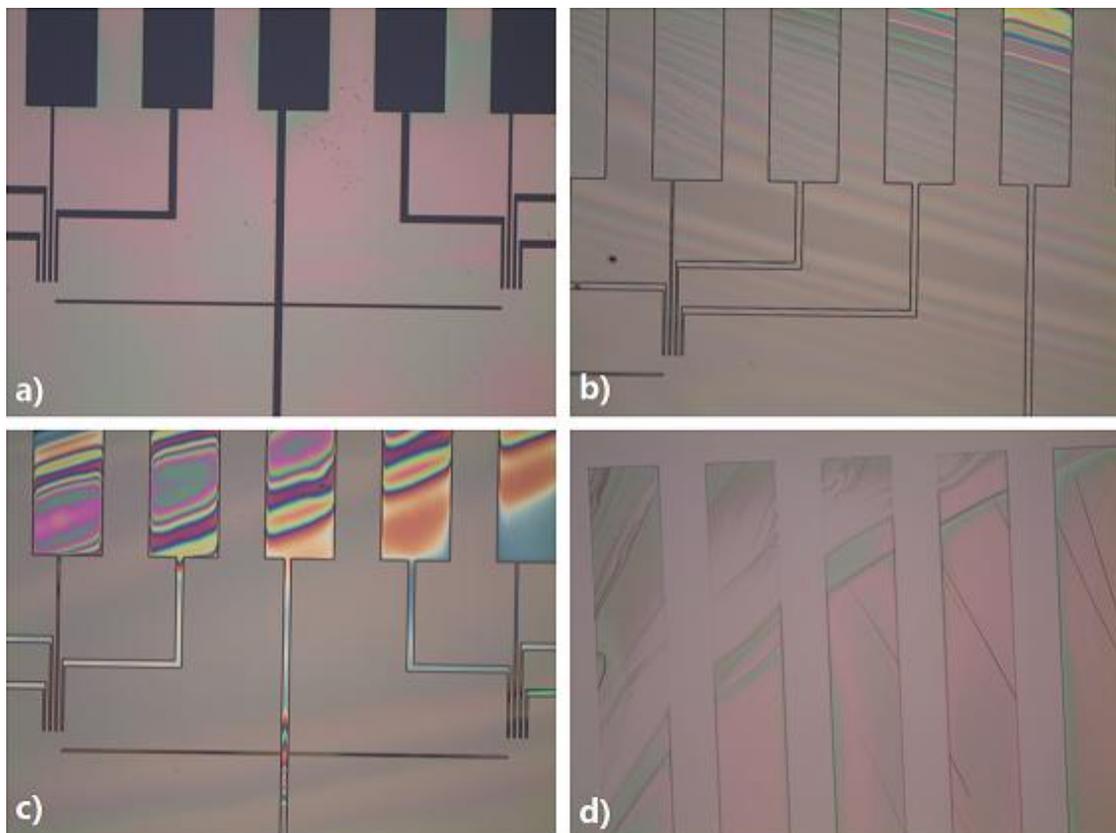


Fig.4.1.3: Optical microscope images of the patterns formed by photolithography with different UV exposure time: a)1.8s; b)2.2s; c)2.6s; d)3.0s. The amplification factor is 50x.

Since mask1 also have the gate pads pattern which is overlap with mask2, I invented a novel method: use the photolithography with mask2 to form the etch mask firstly. Next, etch the holes to doped Si layer. Then, do the photolithography with the mask1 to form not only the electrical connection to source and drain, but also the gate pads. Finally,

deposit metal and lift-off to form the construction. In this way, only one time of metal deposition and lift-off process is needed. (More details please check the appendix C and D, the old and improved photolithography are enclosed.)

After the recipe is designed, it is tested to find suitable parameters. For example, the exposure time is optimized first. With four groups of test (1.8s, 2.2s, 2.6s and 3.0s), I found the best exposure time is 1.8s, as the pattern formed by photolithography is the sharpest. (Shown in fig.4.1.3)

The metal deposition is carried out in Cryofox Explorer 600, in which titanium and gold has been deposited by electron beam evaporation. And the parameters of the deposition are shown below:

Table 4.1: parameters for metal deposition

	Layer1	Layer2
Materials	Titanium	Gold
Base pressure(mbar)	3×10^{-5}	3×10^{-5}
Thickness(nm)	10	50
Rate(Å/s)	2,0	2,0
Pocket No.	4	1
Tooling factor	87	71

Notes: a) Pocket No. is used for selecting the materials to be deposited, No.4 refers to Titanium, while No.1 indicates gold; b) Tooling factor works as a correcting factor in order to get more flat and uniform thickness of materials. According to different materials, it has different range of value, for example, E_{Ti} : 87~84 and E_{Au} : 71~70

When the whole process has been finished, wafer has to be diced into 10mmx8mm chips. The dicing saw equipment is Disco DAD-2H5, and the recipe is shown in appendix E.

Before dicing, photoresist as protective coating is applied to avoid particles on the surface and removed later by acetone.

4.2 Electron-Beam Lithography (EBL)

To fabricate the transistors, large area pattern is formed by photolithography, but the nanoscale electrodes are fabricated by EBL, as the minimum line width that can be achieved with standard contact lithography is around 1 μm .

Compare to photolithography, EBL has higher resolution. However, it takes more time and the process is more complicated. For instance, it calls for coordinate transformation and write-field calibration. Moreover, it needs to set the exposure parameters, such as dose factors. The main procedure is shown below in fig.4.2.1, and more details are presented in appendix F: the step by step procedure of EBL.

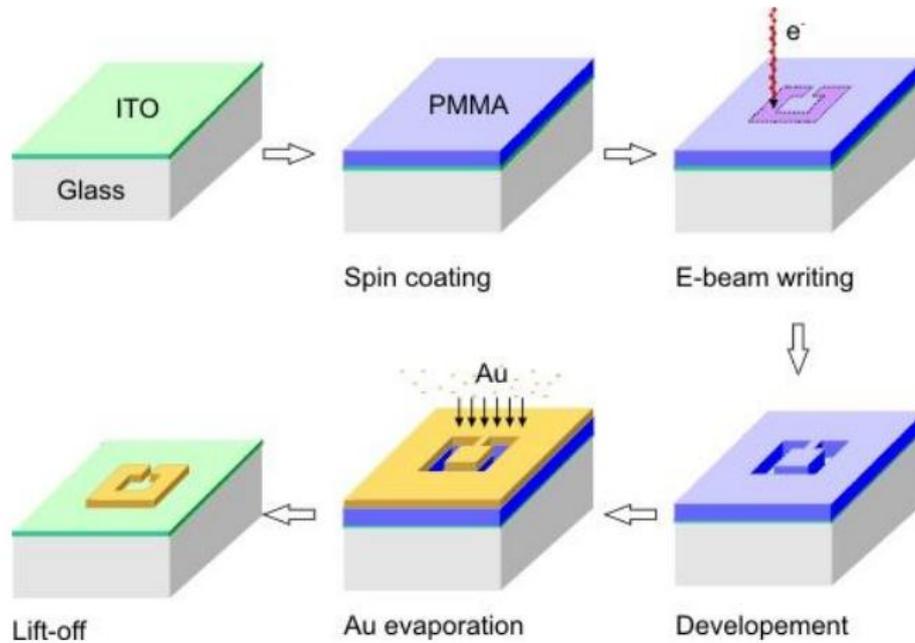


Fig.4.2.1: illustration of the main procedure of e-beam lithography

As for the electrodes design, it is drawn through Raith NanoPECS software, and the distance between the electrodes is 200nm, as this distance is suitable for the in-situ growth nanofibers to cross the electrodes and form the transistor.³⁶

4.2.1 Dosefactor Test

Generally, area dose is related to how many electrons are required to hit the e-beam resist and form the designed pattern with high resolution. In another way, it is used to determine the exposure time according to the beam current. If the value of area dose is higher, a longer exposure time is required. The area does can be calculated by the following equation:

$$\text{AreaDose} = \frac{I_{\text{beam}} \cdot T_{\text{dwell}}}{s^2} \text{ (unit is } \mu\text{As/cm}^2\text{)} \quad \text{(Equation 4.1)}$$

Where I_{beam} is the beam current, T_{dwell} is the dwell time or exposure time, and s is the step size.

Area dose is influenced by many factors, such as the properties of resist, substrate and acceleration voltage etc. So usually it needs to multiply a factor to get the actual value according to different experiments.

In this project, the area dose of SEM has been determined to $310\mu\text{As}/\text{cm}^2$. In order to confirm the dosefactor to get high resolution, several tests with different dosefactors are required.

I fabricated the first group of chips with N3 silicon wafer (the thickness of SiO_2 is 100nm), by EBL. At that time, e-beam resist PMMA A4 is still fresh, so I just tested three different dosefactor, 1.1, 1.2 and 1.3. And the results were pretty good, even dosefactor 1.3 seemed to be a bit over exposed.(The results are shown in fig.4.2.2)

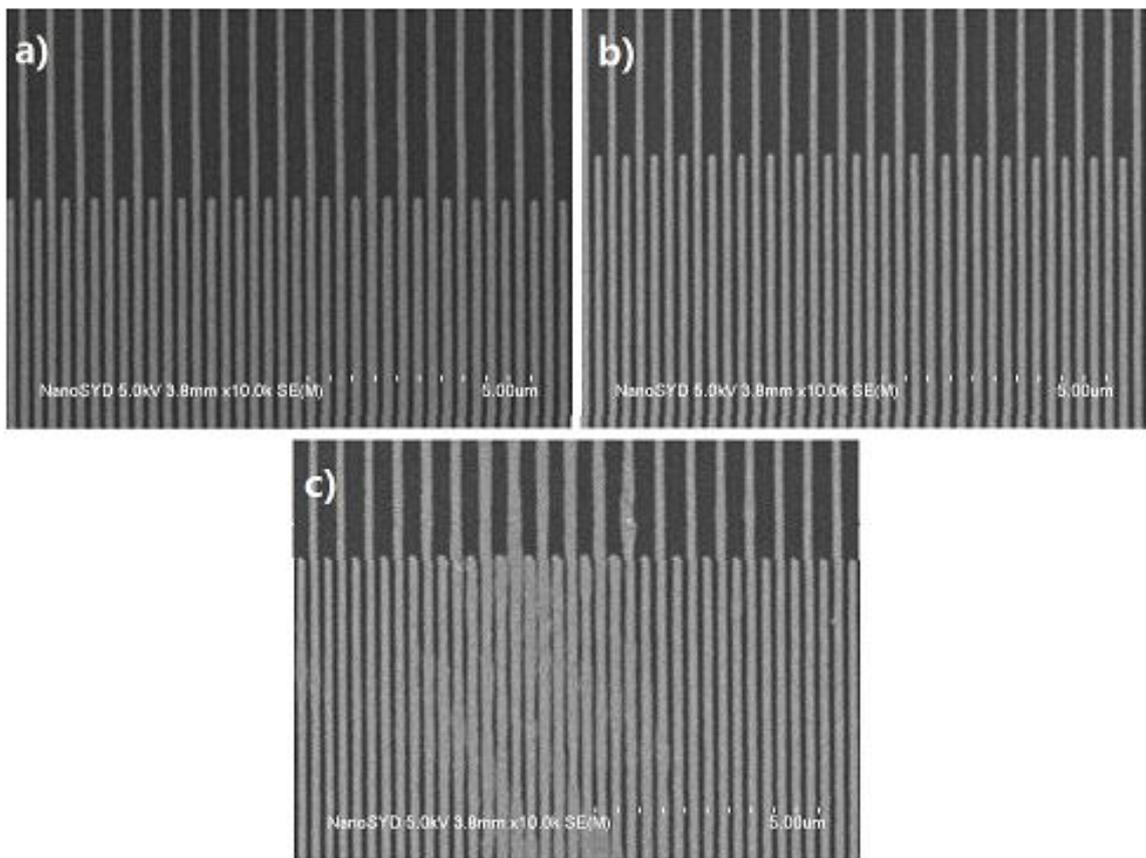
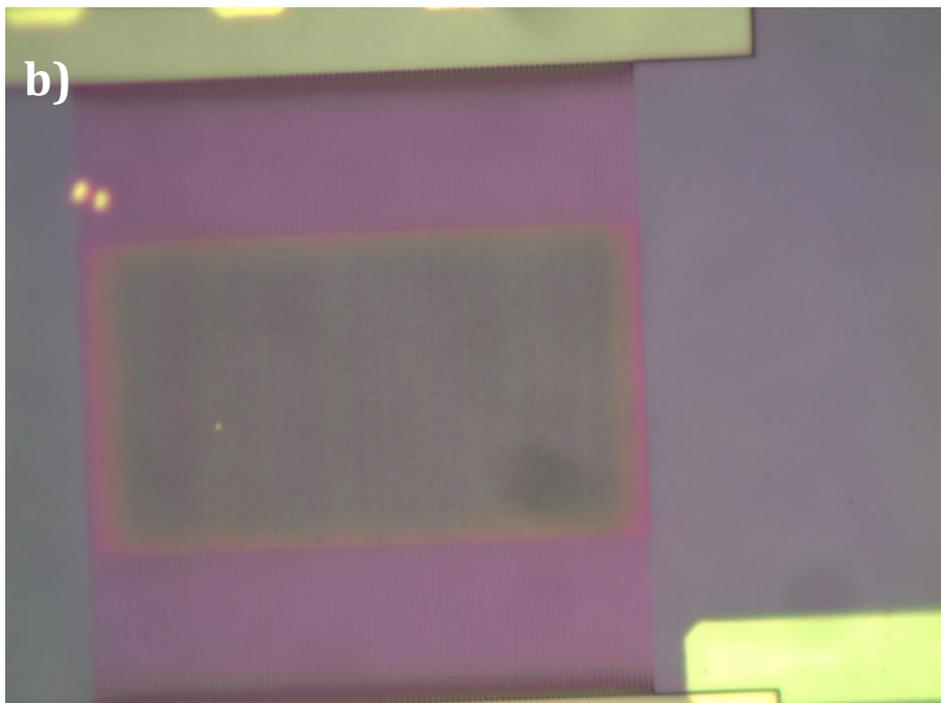
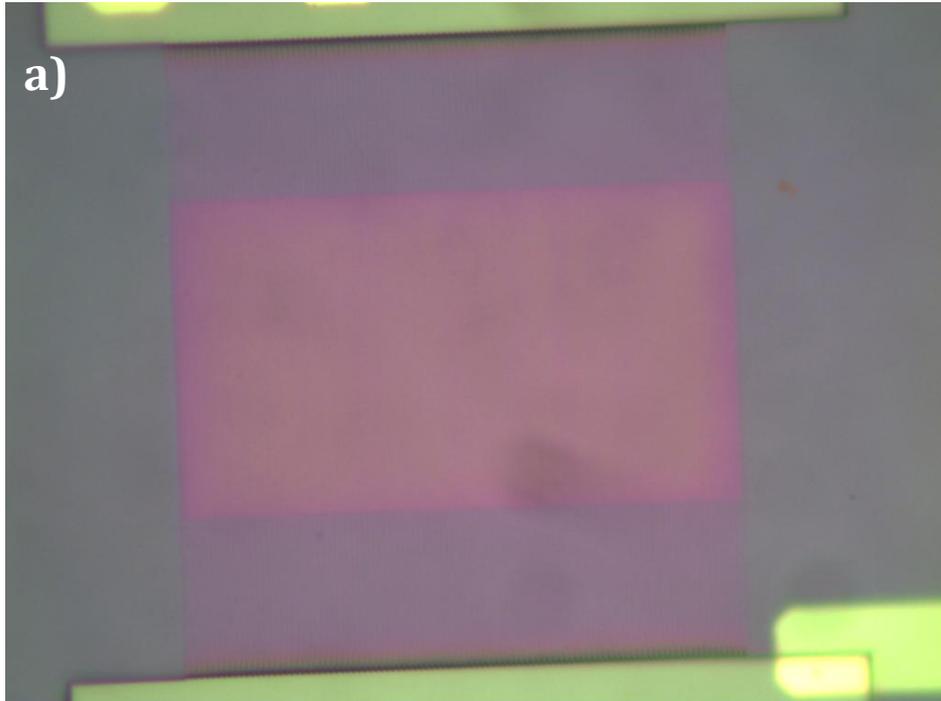
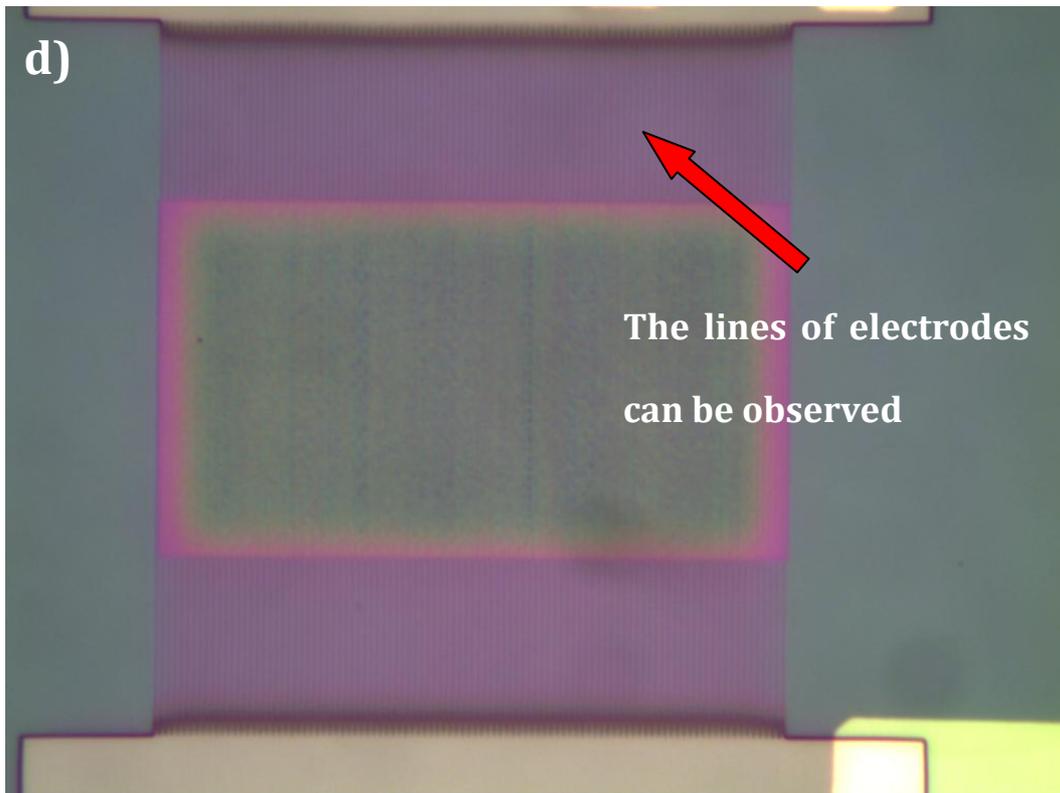
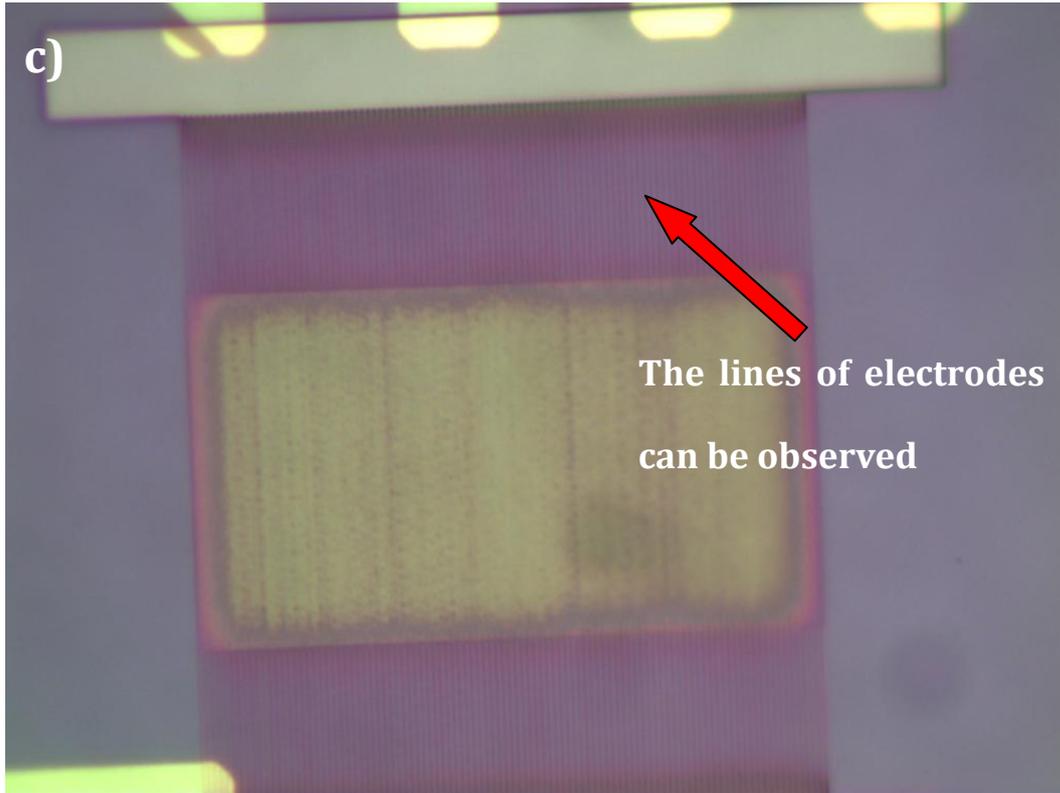


Fig.4.2.2: a) SEM image of the electrodes after metal deposition with dosefactor 1.1; b) SEM image of the electrodes after metal deposition with dosefactor 1.2; c) SEM image of the electrodes after metal deposition with dosefactor 1.3.

However, the first group of chips was not suitable as there was the current leakage through the gate dielectric layer according to the electrical test. The second groups of chips were fabricated with N4 silicon wafer (SiO_2 thickness is 200nm). Unfortunately, at that period, PMMA A4 was out of date, which directly affected the resist properties.

In order to get a better result, I chose PMMA A7 as the e-beam resist. And I test a series of dosefactors: 1.4, 1.5, 1.6, 1.7, 1.8, and 1.9 (shown blew in fig.4.2.3).





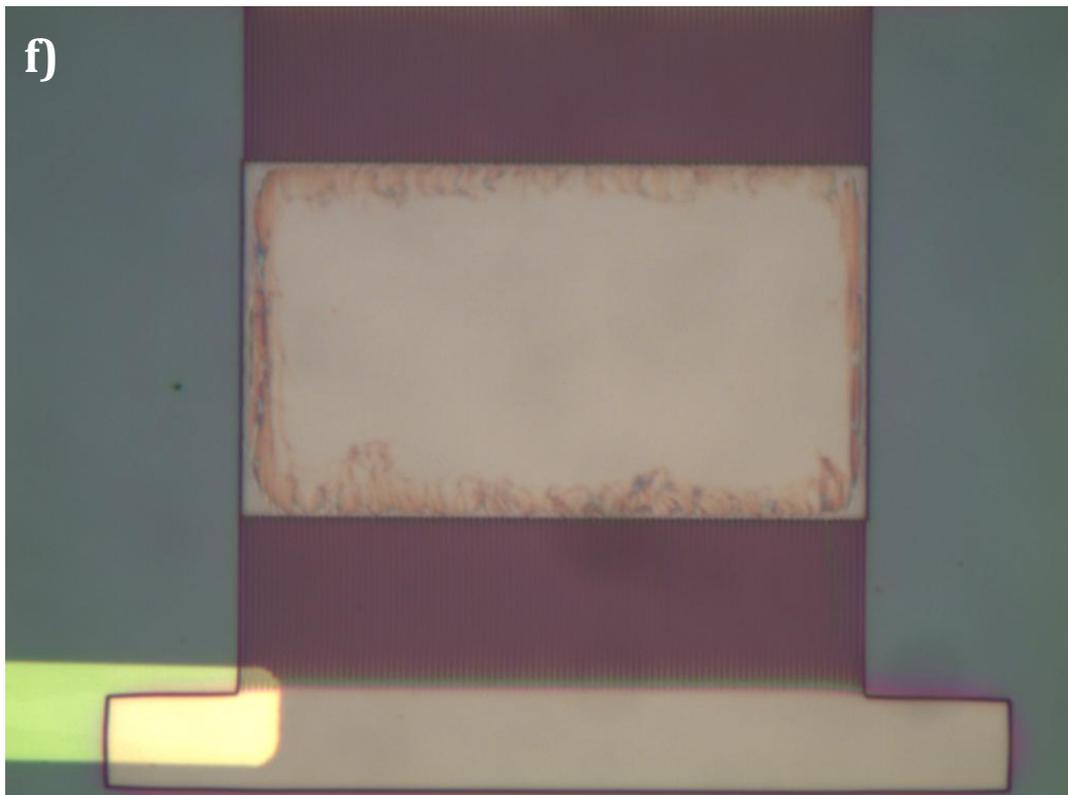
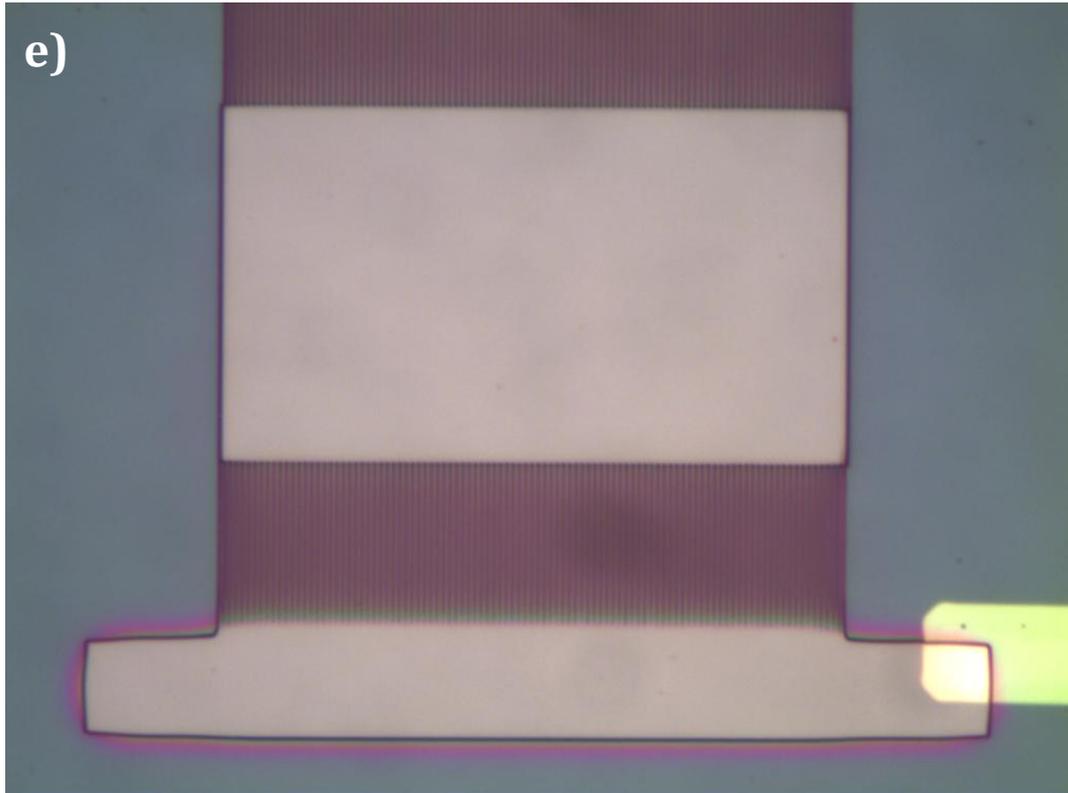


Fig.4.2.3: optical microscopy images of EBL samples after developing with dosefactors: a)1.4; b)1.5; c)1.6; d)1.7; e)1.8 ;f)1.9. The amplification factor is 1000x.

By comparing these images, it is obvious that, the image of dosefactors1.4 is not very sharp, while the images of 1.5, 1.6 and 1.7 have the sharp patterns.

However, the resists seems to be over exposed in the images of 1.8 and 1.9, and after metal deposition and lift-off process, the metal electrodes were found to be merged together (shown in fig.4.2.4).

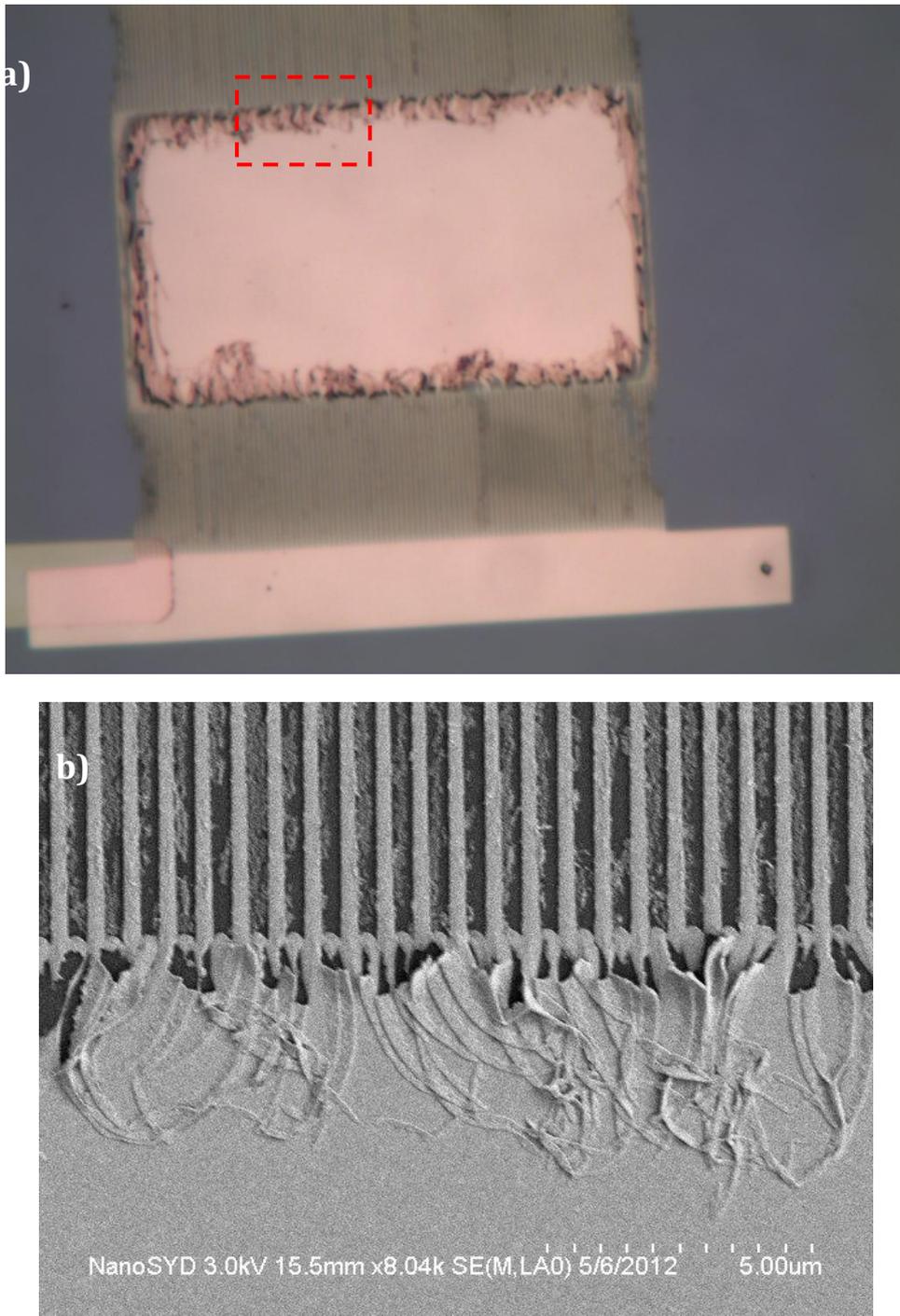


Fig.4.2.4: EBL sample with dosefactor 1.9 after metal deposition and lift-off: a) optical microscope image of the sample; b) SEM image of the red dash line marked area in (a)

4.2.2 Issues and Solution in EBL

However, even found the suitable dose factors (1.5, 1.6 and 1.7), after the metal deposition and lift-off, the electrodes on these samples were still washed away.

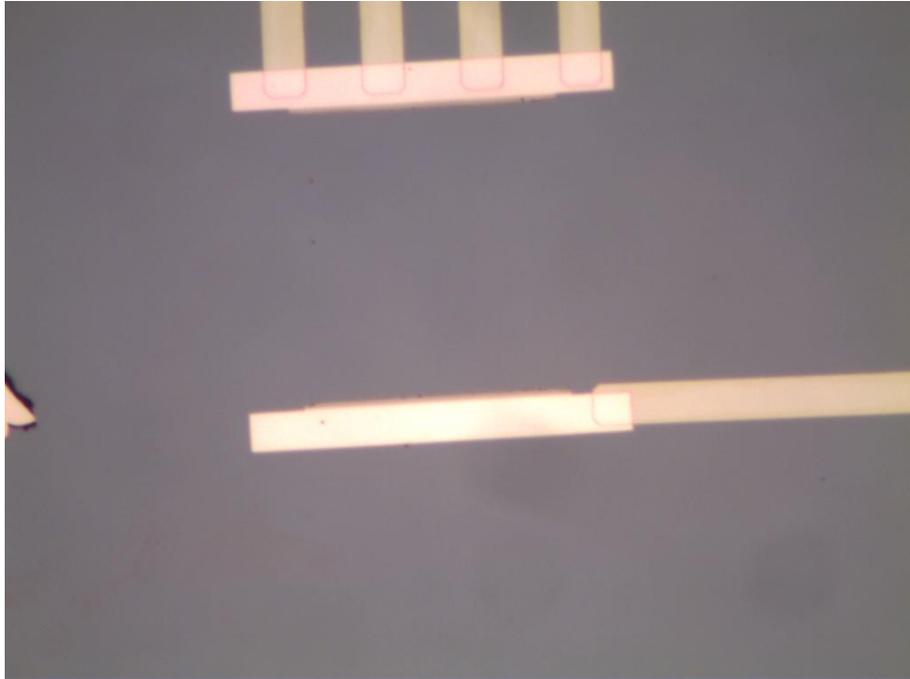


Fig.4.2.5: optical microscopy image of EBL sample with dose factor 1.7 after lift-off. The amplification factor is 500x.

That is probably because there was still some residual PMMA on the surface after developing. So during metal deposition, the metal was deposited on the residual PMMA surface instead of the substrate surface. After lift-off, the metal was washed away with PMMA, as it could not attach to the SiO_2 surface.

And the probably reasons leading to the residual resist could be:

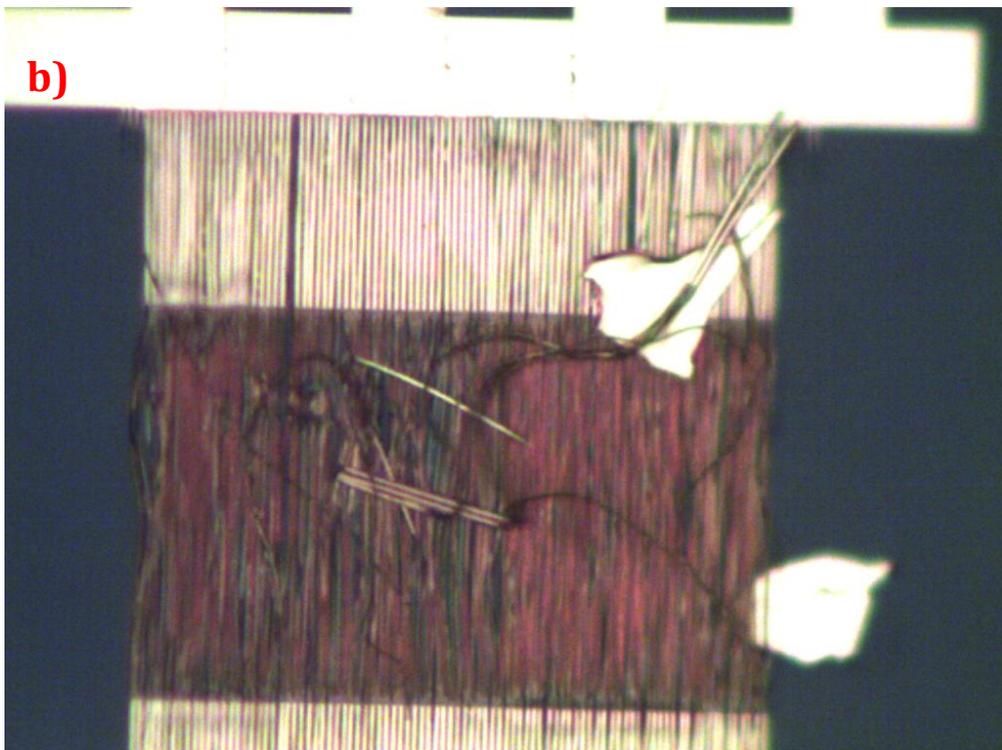
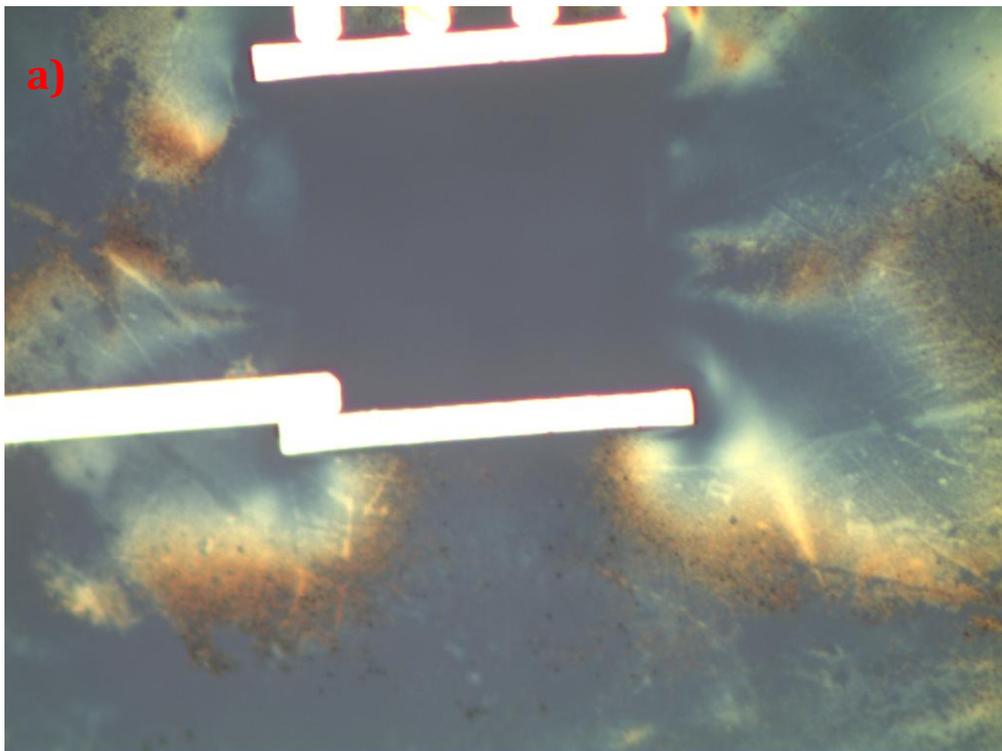
- a) e-beam resist PMMA A7 was also out of date;
- b) As the viscosity of A7 is higher than that of A4, in order to get the same thicker resist (around 200nm), A7 requires high speed in spin coating process.

According to these reasons, there are three solutions:

- 1) Increase the spin speed, in order to get thin PMMA resist coating. (Since the samples had already spin-coated and baked, so I did not choose this solution)
- 2) Extend the developing time. (This method I have already tried, but the effect is not obvious)
- 3) Using oxygen plasma etching to remove the residual PMMA resist.

Based on solution 3, new samples after EBL with dose factor 1.7 and developing were applied with oxygen plasma etch under the same etch power: 100W, but different etch

time (10s, 30s and 60s). Then, after metal deposition and lift-off, the results are shown below, in fig.4.2.6:



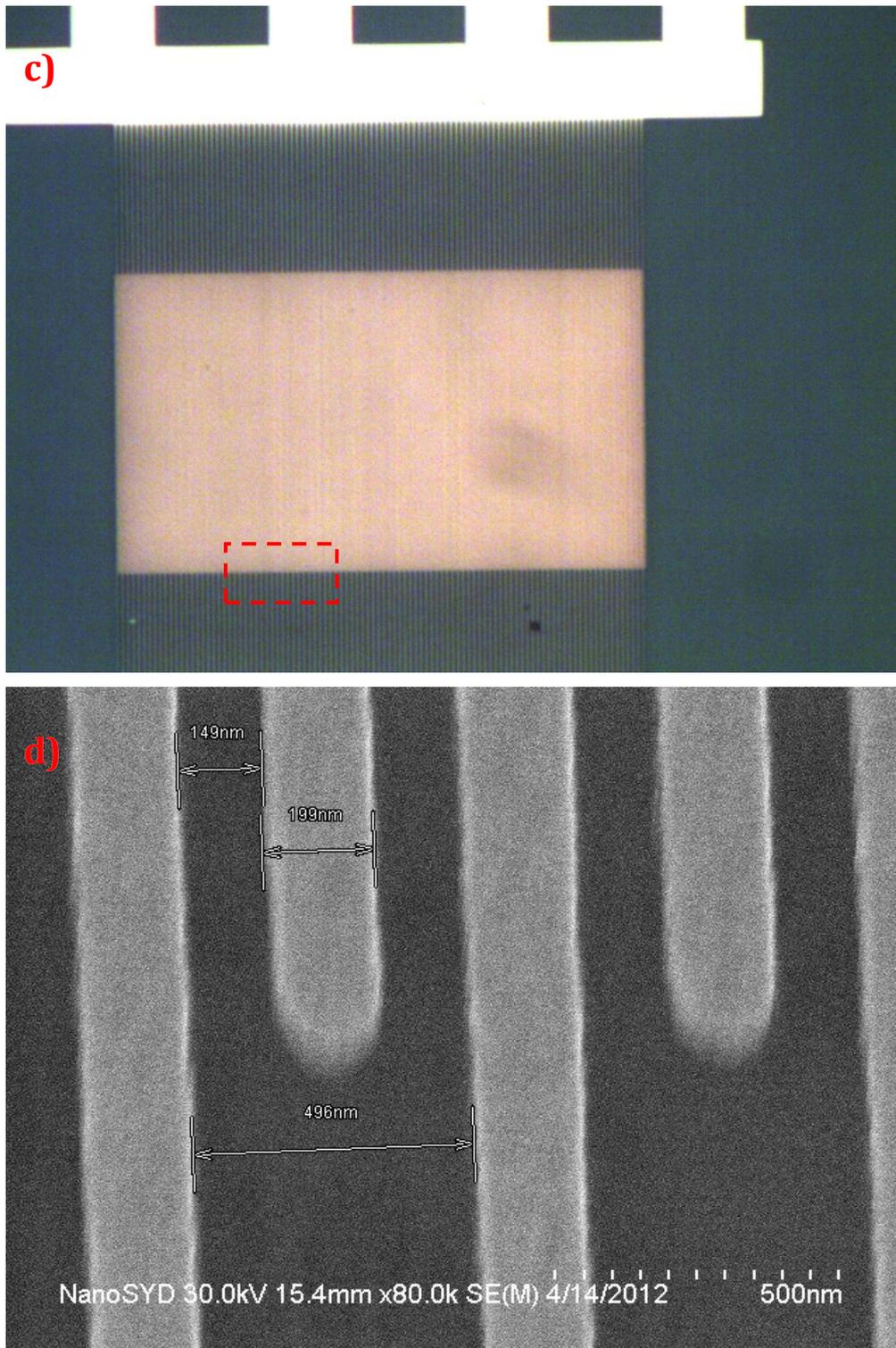


Fig.4.2.6: samples after metal deposition and lift-off, with different oxygen plasma etch time: a) optical microscopy image of sample applied 10s etch time; b) 30s etch time; c) 60s etch time; d) SEM image of the area marked by red dash line in (c). The size of electrodes and the distance between electrodes were measured. (a) was taken with amplification factor 500x, while (b) and (c) with amplification factor 1000x.

It is obviously that the sample of dosefactor1.7 with oxygen plasma etch process under the etch power 100s and etch time 60s, can form the perfect electrodes.

4.3 PPTTPP Nanofibers Growth on Structure Devices

After the fabrication of the transistor substrate, these samples have been applied short circuit test on probe station (more details please check appendix I). If there were not current leakage through gate dielectric layer, samples were put into the vacuum chamber to grow the PPTTPP nanofibers. The procedure and suitable growth condition have been shown in section 2.2.3. The results are shown below in fig.4.3.1. In these images, it is obviously to see the in-situ growth nanofibers crossing the electrodes and forming the transistors.

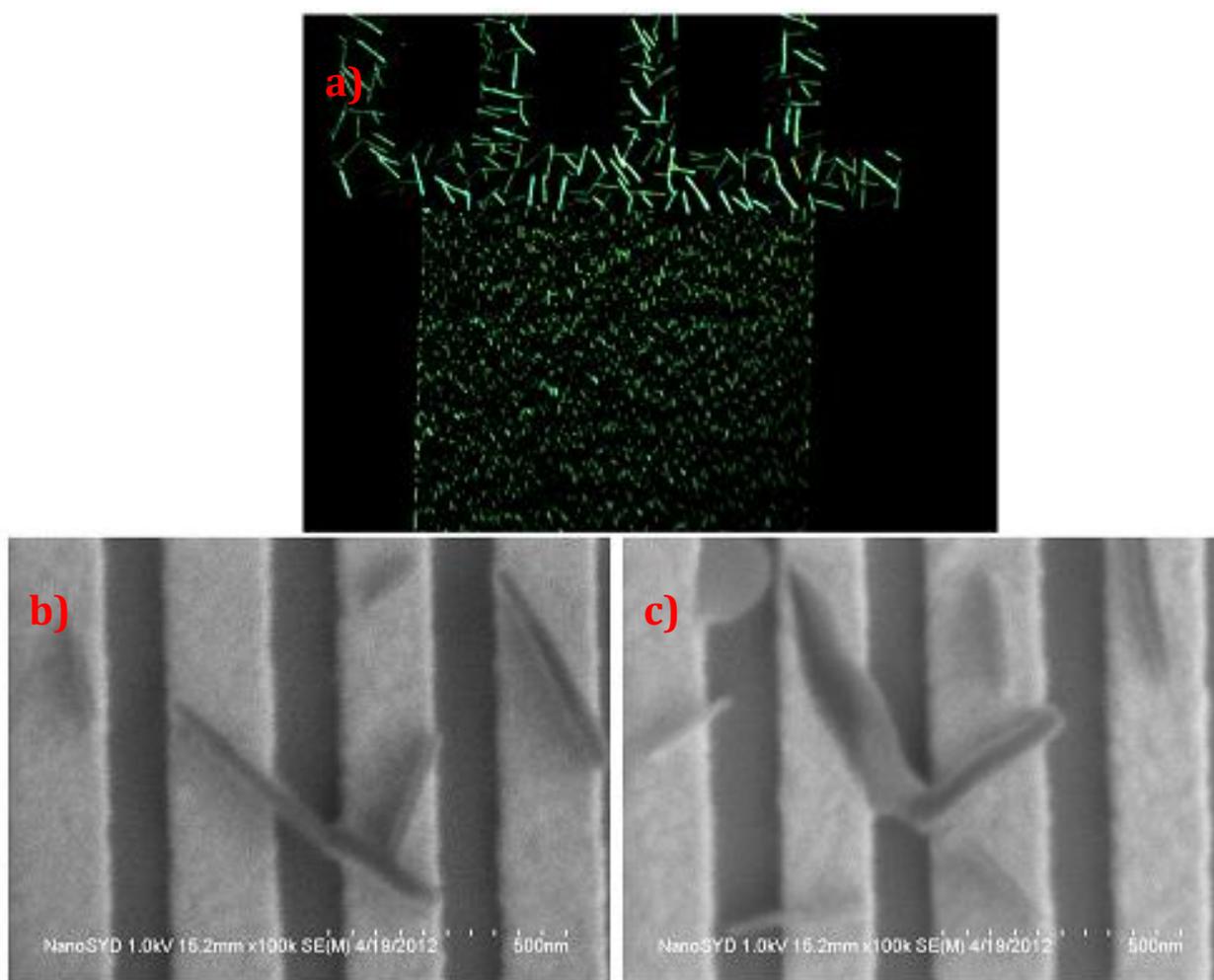


Fig.4.3.1: a) fluorescence microscope image of PPTTPP nanofibers on electrodes with amplification factor 1000x; b) and c) SEM image of in-situ growth PPTTPP nanofibers crossing the electrodes.

In addition, it is important to note that before the deposition, the sample has to be cleaned. As the organic residual and dusts on the samples surface will influence the nanofibers growth, which is attributed to the surface energy of the sample affected by these contaminations.

In order to clean, the sample firstly rinse in acetone for 4~5 minutes. Then rinse in IPA (2-propanol) for 4~5 minutes. Both of these steps are carried out in the ultrasonic tank. After that, the sample has to be rinsed in water for 3~4 minutes, followed by blow dry. Finally, the oxygen plasma etch is applied with power 100W and time 60s.

A contrast experiment has been made, through the fluorescence microscope. It is not difficult to find the nanofibers growing on the unclean sample are much shorter than these growing on the clean sample.

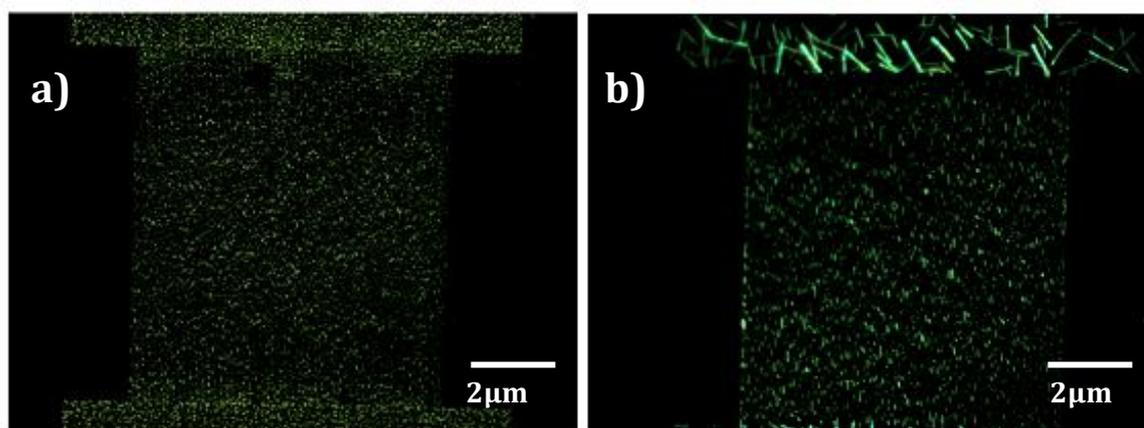


Fig.4.3.2: fluorescence microscope image of PPTTPP nanofibers on growing on a) unclean sample; b) clean sample.

4.4 How to Remove PPTTPP Nanofibers from Transistor Substrates

As we know, the processes of fabricating the transistor substrate are complicated and the whole procedure takes a long time. Moreover, it also costs lots of money. So how to reuse the substrates, which have already deposited organic nanofibers, becomes an interesting topic. However, these organic materials are difficult to dissolve in many solvents, so it is not easy to remove these materials from the substrate surface.

After several groups of test, I found oxygen plasma etcher can easily remove the organic nanofibers without or less damaging the electrodes and substrate. The oxygen plasma etcher I used is Branson IPC 3000, which usually is used to etch organic films and residues such as photoresist. It also can be used to active the polymer materials.

Oxygen plasma etch was applied to the test sample with the etch power 100W. As the etch time increased, it was obvious to see the nanofibers on the surface of electrodes disappearing.

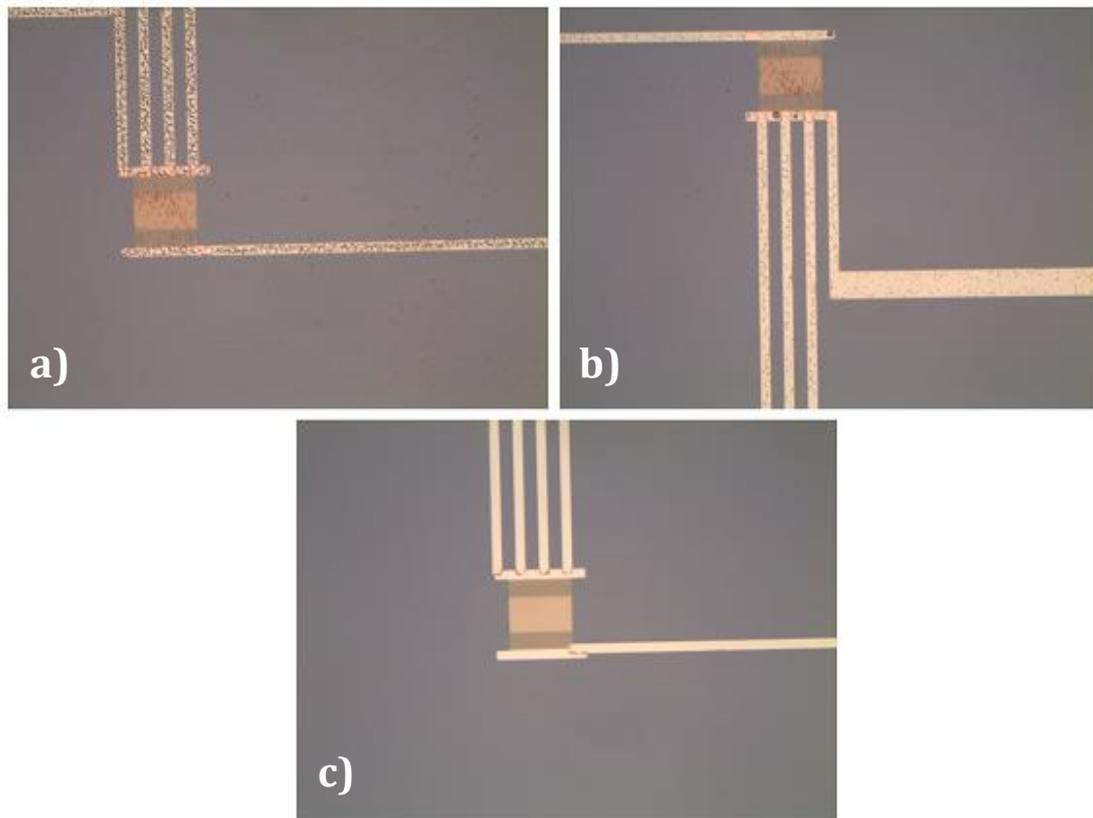


Fig.4.4.2: optical microscopy images of the electrodes after different oxygen plasma etch time: a) etch 0s; b) etch 60s and c) etch 90s. The amplification factor is 200x

Based on the optical microscopy images and electrical test (more details about electrical test please check appendix I), the PPTTP nanofibers can be removed from the used samples without damaging the electrodes by applying oxygen plasma etch with power 100W and etch time 90s.

Chapter 5 Light Emission Experiment

Based on the theory in section 3.5, emission intensity measurements carried out. In this chapter, the set up and procedure of intensity measurements will be described first, including the preparation, such as wire binding. Since the experiment is operated by AC gate voltage, so the relation between light intensity and gate voltage, as well as the relation between light intensity and frequency of gate voltage will be discussed. Finally, the damaged samples will be presented and the reason will be analyzed.

5.1 Experimental

Before the light emission experiment, the samples need some preparations, such as wire bonding, in order to create electrical connection from the chip to the electrical circuits.

Wire bonding was carried out on the equipment K&S 4500 series manual wire bonders using the wedge type of wire bonding.

When doing the wire bonding, some accidents happened, such as the wire breaking. As a result, the wire should be passed through the needle and hole again. That is a tricky part, as the hole at the tip of needle is difficult to see. So it calls for lots of patience and stable manual operation. The trick is when passing the wire through the needle, you should press “Test” bottom to make use of the ultrasonic vibration to “suck” the wire into the needle. When passing wire through the hole, send the wire to the hole from upper direction. And a good tweezers would make this work easier.

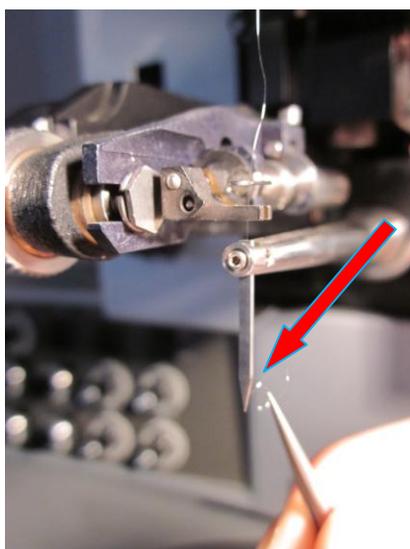


Fig.5.1.1: illustration of how to pass the wire through the hole. The red arrow indicates the direction to send the wire passing through the hole

After the wire bonding, the sample is ready to do the light emission experiment. The optical experiment is based on the principle mentioned in section 3.5.2. The source and drain electrodes are connected to DC voltage supplies. In this project, the DC voltage is 0V. AC sine voltage is applied to the gate electrode by a digimess FG100 Function Generator with a Falco Systems voltage amplifier. The AC function generator is connected to computer.

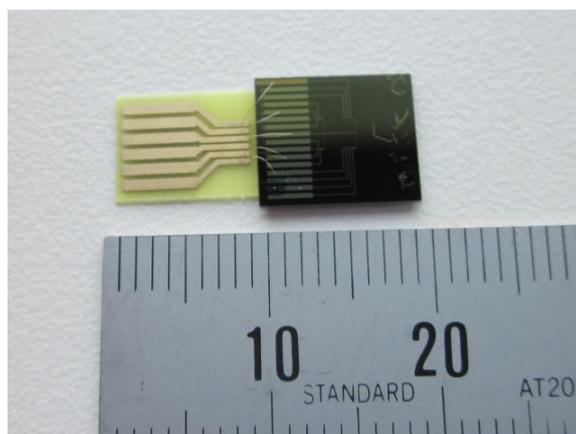


Fig.5.1.2: image of the sample after wire bonding

The sample is placed in vacuum chamber. In this way, the life time of the sample will be extended and it also makes the light emission easily be observed. The emitted light through the window on the chamber is collected by a $\times 20$ objective lens and captured by Andor camera. The camera is also connected to the computer. The whole setup is shown below, in fig.5.1.3.

Place the sample into the vacuum chamber and pump down the chamber first. Then integrate the sample into the circuit as shown in fig.5.1.3. Next, adjust the microscope to focus on the sample, and turn on the function generator, amplifier and DC voltage supplier. After that, set exposure time of the camera as 3s and sweeping range for amplitude or frequency of AC gate voltage, and step size. Finally, turn off the light and start the light emission measurements.

The whole process is operated by the Labview program. By sweeping voltage or frequency, the camera will take the images automatically when the voltage or frequency reaches to the pre-set values.

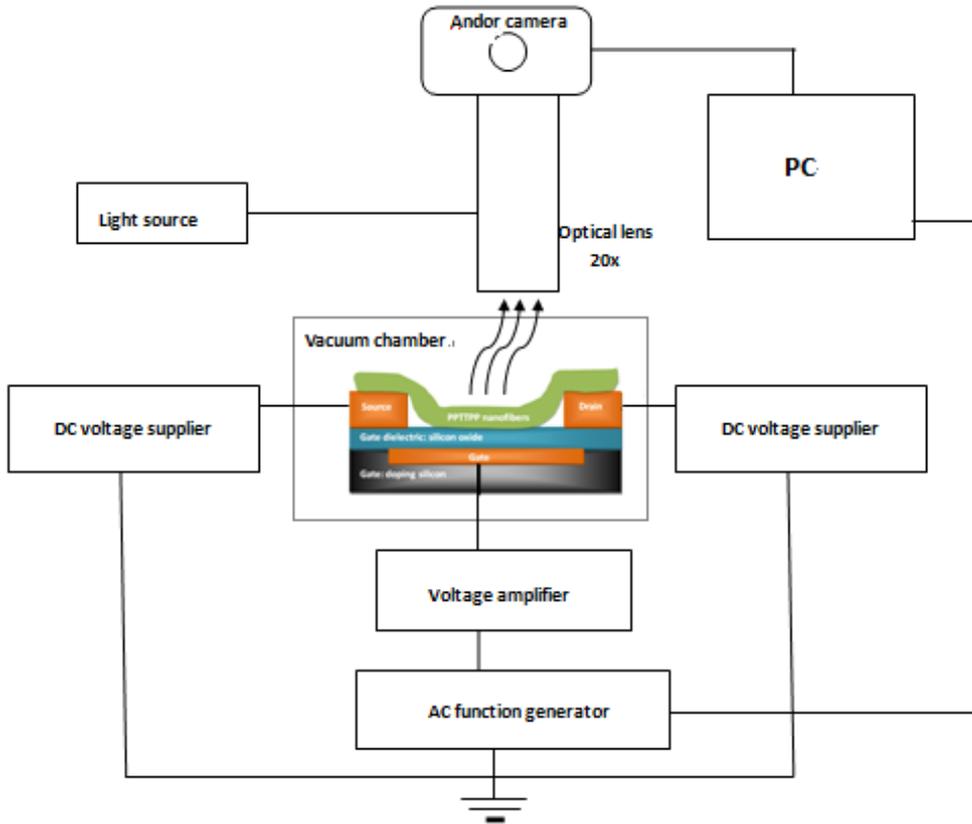


Fig.5.1.3: Schematic diagram of the light emission experiment setup

5.2 Results and Discussion

5.2.1 Gate Voltage Dependent Light Emission

In order to find how the gate voltage affects the light emission, the following experiment is carried out. The range of amplitude of gate voltage was sweeping from 1.0V to 3.6V, with a step of 0.2V. However, after the amplifier, the actual amplitude of gate voltage ranged from 25V to 90V. The frequency was constant value at 250 kHz. During sweeping, the images were saved by Andor SOLIS software. The images are shown below in fig.5.2.1. Obviously, the light emission is increased according to the increased gate voltage amplitude.

In order to prove this conclusion, these images are input into the matlab program (Appendix G). Through this program, 20 points in the light emission area of each image were selected to measure the emission intensity. The unit of intensity is a.u., which means arbitrary unit, as the intensity values are relative values after comparing the max and min intensities of all the images.

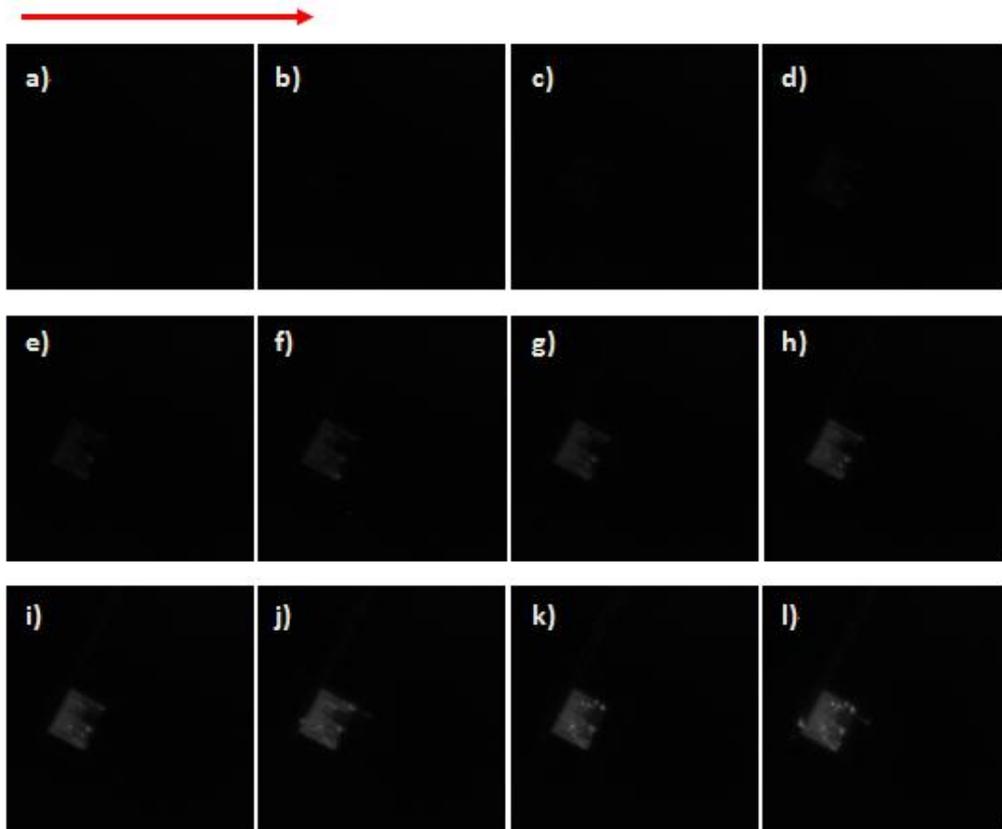


Fig.5.2.1: light emission images taken from the OLET, by sweeping the AC gate voltage, the amplitude of the gate voltage from 30V (a) to 90V (l). The frequency is 250 kHz. According to the red arrow's direction, the voltage is increased. At the gate voltage amplitude is 25V, the light emission is invisible, so the image is not added into this image group.

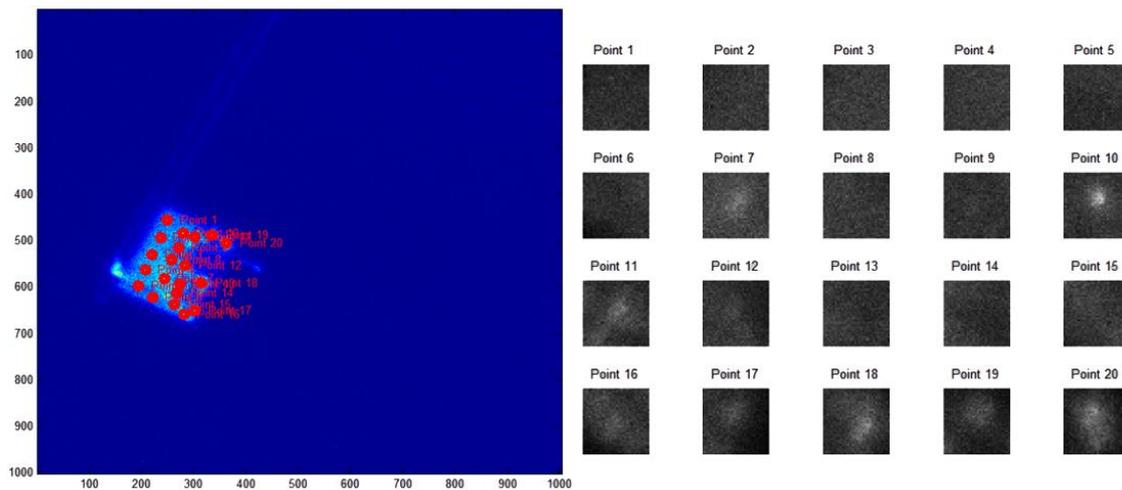


Fig.5.2.2: a) 20 points have been selected in the light emission area of the sample before the measurement; b) the images got from each point

In these points, maximal and average values of light emission intensity were measured individually. Based on these values, two series of curves were obtained. (Shown in fig.5.2.3)

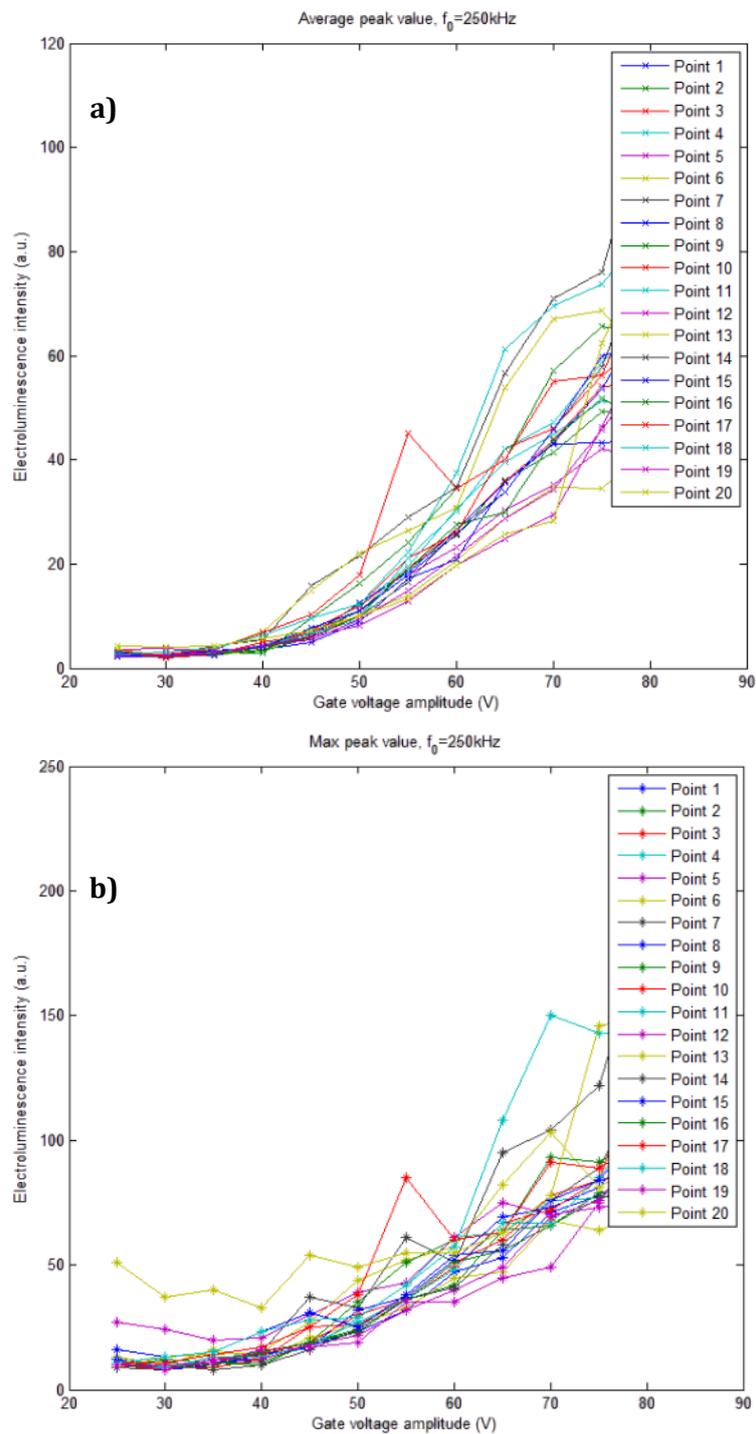


Fig. 5.2.3: a) average values of light emission intensity from each point according to the increasing gate voltage amplitude; b) max values of light emission intensity from each point according to the increasing gate voltage amplitude

According to these data from 20 points, the average value of luminescence intensity from all the points can be obtained forward. Finally, we can get:

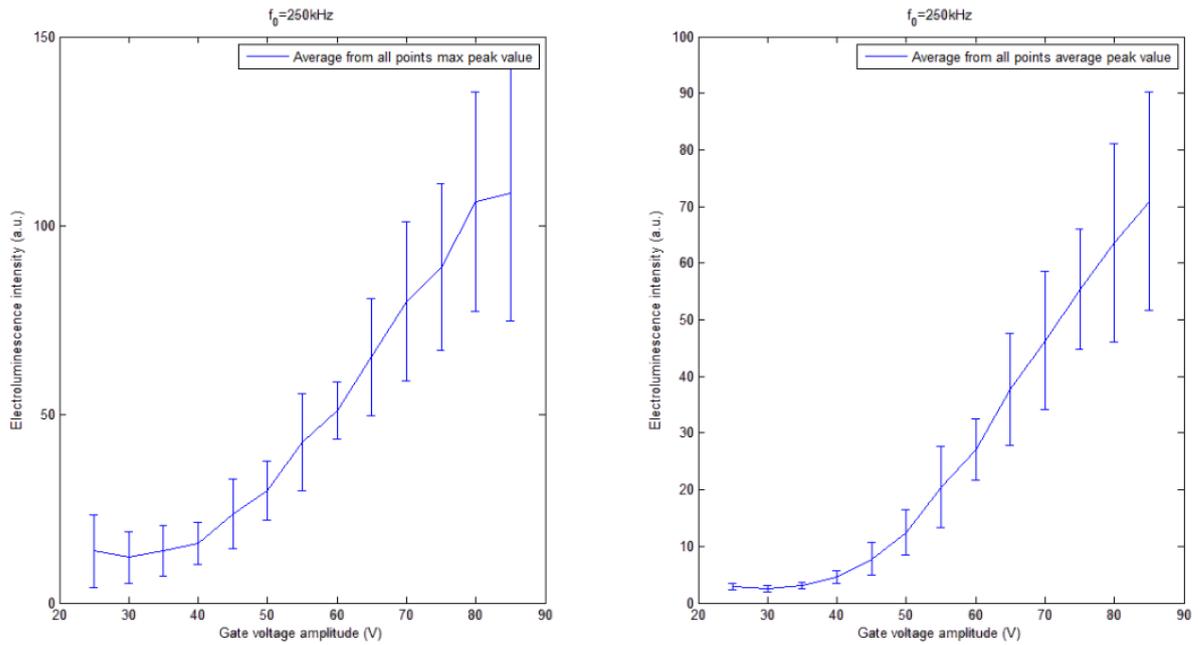


Fig.5.2.4: average value of 20 points luminescence intensity according to the increasing gate voltage amplitude.

Based on these curves, it is not difficult to see that the luminescence intensity of the transistor is increased according to the increased amplitude of AC gate voltage. The reason is as the voltage increasing, more charge carriers are injected into the semiconductor, and the charge carries mobility is increased. All of these will increase the possibility of the recombination of holes and electrodes. As more holes and electrodes recombined together and emit photons. So the intensity is increased (as discussed in section 3.5.2). However, due to the curves, the light intensity and the amplitude of AC gate voltage are not followed a simple liner relationship, so in order to derive the function between intensity and amplitude of voltage, more measurements and calculation are needed. Due to the time limit, this cannot be done in this project.

Moreover, the error bars in the curves are relative large, which means the light emission is not uniform in the sample. This is probably because of the contact condition between nanofibers and metal electrodes. Some nanofibers contact with electrodes in a large area, so more charge carriers can be injected into semiconductors, leading to high emission intensity, whereas some nanofibers contact with electrodes a small area, so the contact resistance is higher, or the injecting energy barrier is higher, so the emission intensity is lower.

5.2.2 Frequency Dependent Light Emission

Similar to last test, the process is almost the same, but sweeping the frequency of AC gate voltage. The amplitude of AC gate voltage kept at 1V, which after amplification was 25V. The frequency was sweeping from 10kHz to 60kHz, with step size 5kHz. The

program to deal with this test is enclosed in appendix H. Likewise, 20 points in the light emission area are taken to measure. The curves of average value and maximum value from each point according to the increasing frequency of AC gate voltage are showed below in fig.5.2.5.

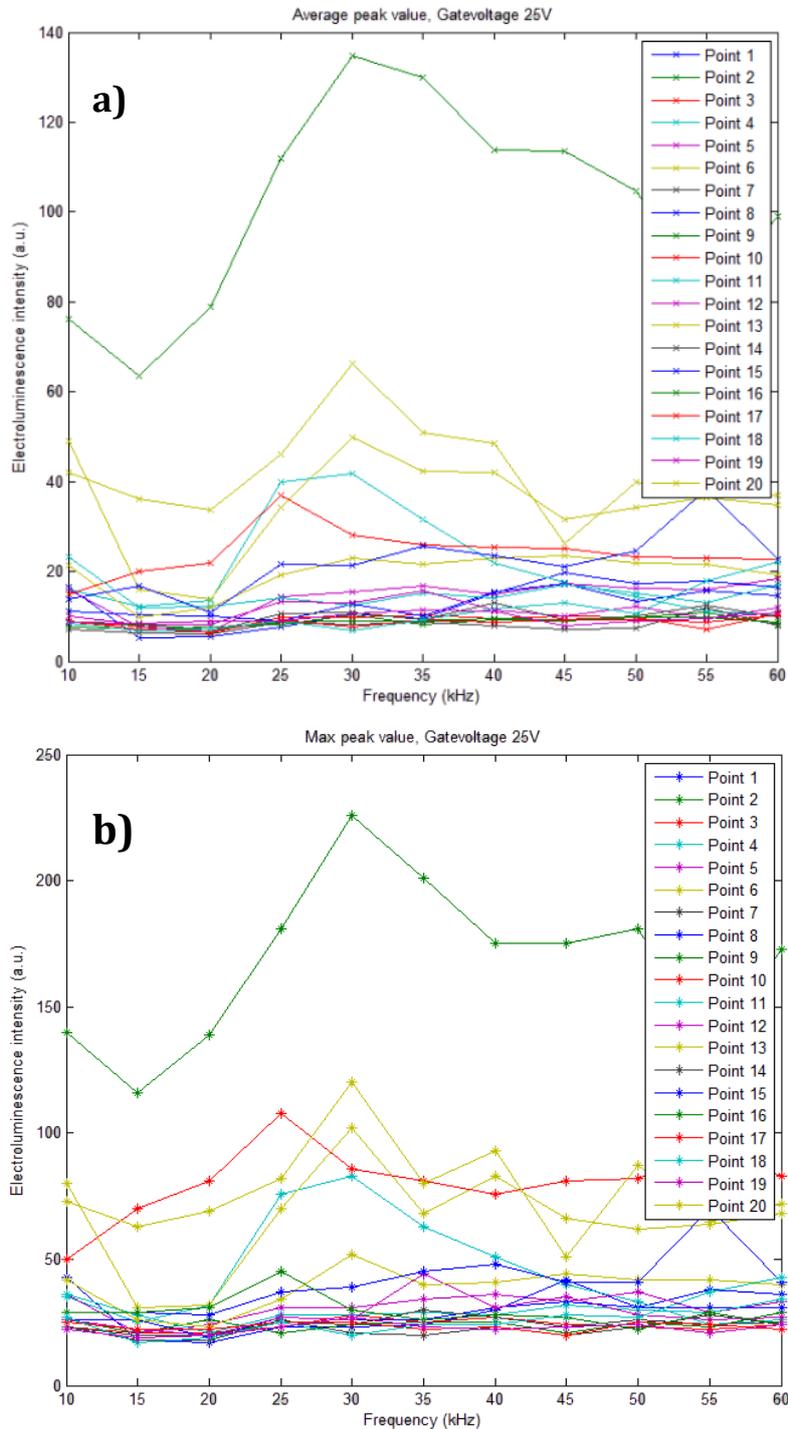


Fig.5.2.5: a) average values of light emission intensity from each point according to the increasing gate voltage frequency; b) max values of light emission intensity from each point according to the increasing gate voltage frequency.

According to these curves, it is obvious that the light intensity of most points are very low, ranging from 0 to 100, except point 8, which ranges from 100 to 230. That is mainly because the sweeping test carried out at relative low AC gate voltage 25V, which is to prevent the chip being damaged during the sweeping test. However, even under this low gate voltage, the chip was still damaged after several tests. (The damaged chips will be shown in next section).

However, based on the average value of these points, the trend of light intensity according to the increasing frequency is still appeared. The intensity of light increase first. When the frequency reaches to around 30kHz, the intensity arrives the maximum value. Then, it decreases a bit and keeps in a stable value when the frequency increased to 45kHz.

The reason for this has also been mentioned in section 3.5.2. The intensity increases first, is mainly because when the frequency increased, which means the shift speed of voltage is increased. So when voltage is positive, electrons are injected from electrodes. When the voltage shift into negative, if the shift speed is fast enough, the injected electrons is still stay in the channel, and meet the later injected holes. As the frequency is higher, so the electrons will meet the holes faster, which means more electrons will meet with holes, so the emission intensity is higher.

However, when the frequency increased to certain value, the intensity of emission light is not increased anymore and keeps in a saturate value. That is probably because of the amplitude of voltage. As the amplitude keeps the same, so the injecting energy is the same, which means the number of charge carries could inject into the channel is almost the same and it is independent with frequency. That is why the intensity reaches to the saturate value at last.

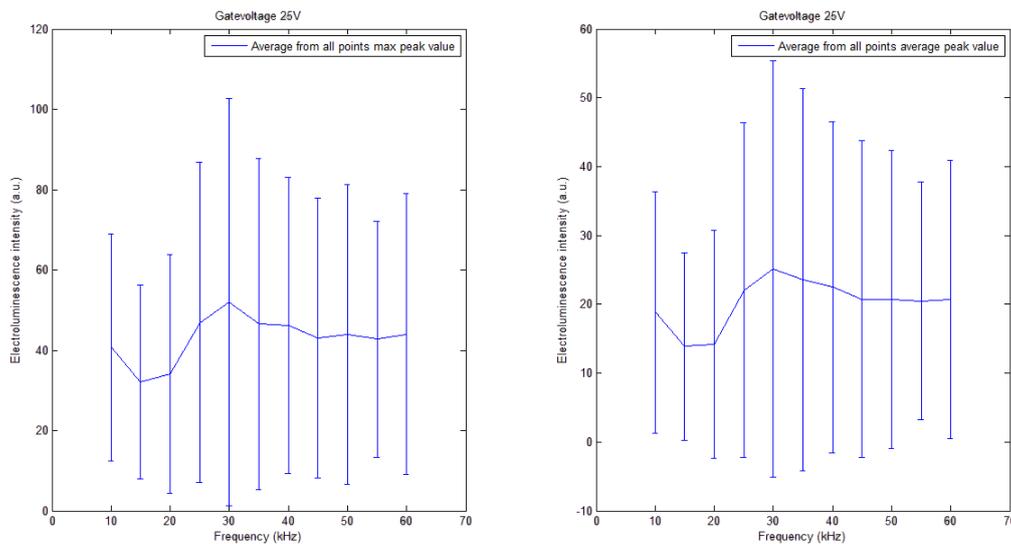


Fig.5.2.6: average value of 20 points luminescence intensity according to the increasing gate voltage frequency.

5.2.3 Damaged Samples

After several groups of sweeping tests, we found the samples being damaged. For example, in voltage sweeping tests, when the voltage is higher than 3.4V with the frequency 250kHz, the electrodes were melted, while in frequency sweeping tests, after several confirming tests from 10kHz to 60kHz with amplitude of voltage at 1V, the electrodes were destroyed too. These samples have been observed through fluorescence microscopy and SEM, which proves the conclusion. The images are shown below in fig.5.2.7:

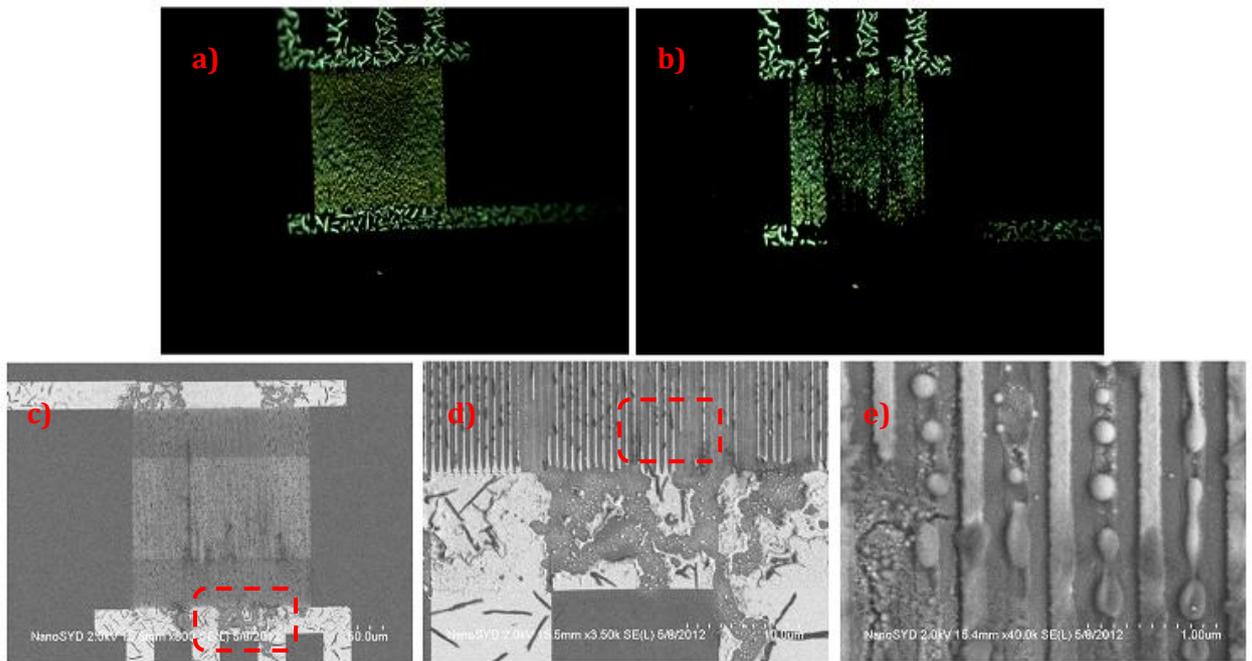


Fig.5.2.7: fluorescence microscope images of the electrode before (a) and after (b) the sweeping test, the amplifier factor is 500x; (c) SEM image of damaged electrodes; (d) SEM image of the damaged area marked by red dash line in (c); (e) SEM image of the damaged area marked by red dash line in (d)

Through the images, it is obvious that electrodes are melted in some parts, and nanofibers are also disappeared in some areas.

The main reason is because of the high charge carrier injecting barrier. So the high voltage is required for the transistor to emit the light. However, as the semiconductor has relatively high resistance, so most of the energy is converted into heat, instead of light emission. Due to the heat, the electrodes are melted. (This has been discussed in section 3.5)

Chapter 6 Conclusion and Outlook

p6P (Para-hexaphenylene) and PPTTPP (5,5'-di-4-biphenyl-2,2'-bithiophene) are two kinds of chain type moleculars with similar structures. Based on proper conditions, they can grow into crystalline nanofibers or thin films on certain substrates, such as mica and gold. The growth is according to the island-layer growth mode. Because of π -bonds between the neighbor molecules and herring-bone crystal structures, these two materials have high anisotropic charge carrier mobility and the fluorescence is polarized due to the high oriented crystal structures.

As self-assembled organic semiconductor materials, they can be applied into organic field effect transistors (OFETs). Usually, there are two ways to integrate these materials into the devices: transfer technology and in-situ growth technology. OFETs are made of three electrodes (source, drain and gate), dielectric layer and semiconductor layer. Generally, the gate controls the carrier movement from the source to the drain.

According to the position of semiconductor layer relative to electrodes and dielectric layer, OFETs can be divided into three types of structure s: BC/BG, TC/BG and BC/TG. While based on the polarity of major charge carriers in the transporting channel, OFETs can also be classified into unipolar OFETs (p type or n type) and ambipolar OFETs. Unlike the inorganic FETs, the transport charge carriers are determined not only by the type of semiconductor materials, but also by the type of metal electrodes, the dielectric layer and the ambient environment.

In OFETs, once positive charge carriers meet negative charge carriers, they will recombine together and emit excitons. Part of these excitons will release energy in the form of photons instead of heat. In this way, the OFETs operate as organic light-emitting field-effect transistors (OLEFETs). Generally, OLEFETs can operate not only under DC gate voltage, but also under AC gate voltage. As for DC gated OLEFET, if it is unipolar charge carried channel, the light emission can only be observed in the area near one electrode, because the only one charge carrier can transport through the channel and meet the opposite charges when they arrived at the other electrode. In this way, light emission is very weak. If it is a ambipolar DC gated OLEFET, since holes and electrons can be injected from respective electrodes at the same time, the recombination efficiency of holes and electrons is improved, so the light emission is much more stronger than unipolar DC gated OLEFET. And the emission zone can move in the channel according to the recombination area. Regard to AC gated OLEFETs, mainly indicate ambipolar OLEFETs. Under AC gated voltage, OLEFETs can even operated when

$V_d=V_s=0V$, as hole and electrons can be injected from both source and drain. With relative high frequency and amplitude of gate voltage, light emission can be observed.

Based on these theories, relative experiments have been carried out. Firstly, due to the deposition experiment, the optimized growth conditions for PPTTPP nanofibers on gold surface have been determined to deposit temperature at 423K, deposit pressure at around 10^{-7} mbar and deposit rate at $0.1\text{\AA}/s$ and the thickness between 5~6nm. Furthermore, the PPTTPP nanofibers have been characterized by SEM, AFM and fluorescence microscope. The static data of the sizes of PPTTPP nanofibers on gold surface have been recorded, and the average lengths for nanofibers growing under 423K, 433K and 443K have been calculated out: $5.7\mu m$, $4.32\mu m$ and $3.10\mu m$, respectively.

Then in the micro-fabrication experiments, photolithography has been applied to fabricate the electrode connection while e-beam lithography has been used to form the nano scale electrodes. During these procedures, a new photolithography procedure has been invented, which can reduce one time of metal deposition. And a method through oxygen plasma etch under 100W and 90s to remove the deposit PPTTPP nanofibers from the substrates has also been found.

After the substrate fabrication and nanofibers deposition, the OLEFETs have been prepared for light emission experiment. In this project, in-situ growth PPTTPP nanofibers on BC/BG type of OLETs have been applied in emission experiment to test out the photoelectrical property of PPTTPP. One test is by sweeping the amplitude of AC gate voltage, while the other test is by sweeping the frequency of AC gate voltage. In both tests, the light emission have been observed and recorded. According to the drawn curves, it is obvious that light intensity is increased according to the increased gate voltage or frequency. However, the relationship between intensity and gate voltage is not simply linear. So the relation function between them cannot be derived. Likewise, the relation equation between frequency and light intensity cannot be derived either. However, many samples after the sweeping tests are destroyed. This is mainly because the high injection barrier, between metal electrodes and semiconductors, leading to the high heat.

Based on these experiments, further works can be carried out in future:

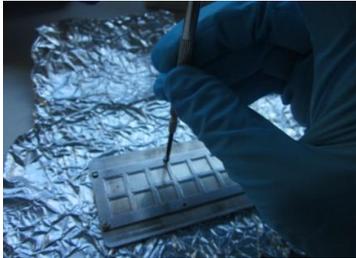
- a) Electrical experiment can be done to measure the electrical property of PPTTPP nanofibers, including the threshold voltage and charge mobilities.
- b) More light emission measurements are required. Based on these data, the relation function between AC gate voltage and light intensity can be derived, as well as the function between frequency of AC gate voltage and light intensity.
- c) The charge injecting efficiency need to be improved. It can be obtained by using two different kinds of materials to fabricate the electrodes, with their energy level

closing to HOMO level or LUMO level individually. The BC/TG structure can also be applied into OFETs, as it can improve the effect of gate. Moreover, special materials can be used as the dielectric layer, to reduce the charge carriers trapping in the dielectric layer.

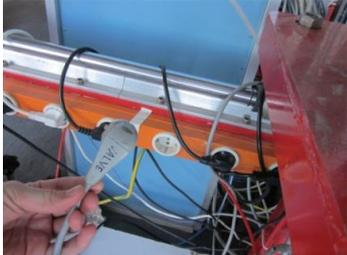
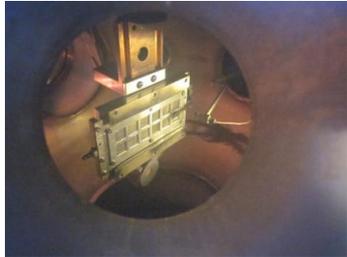
- d) Deposit p6P and PPTTPP nanofibers on the same substrate, active them to emit different color of light, so the multi-color transistor is obtained.

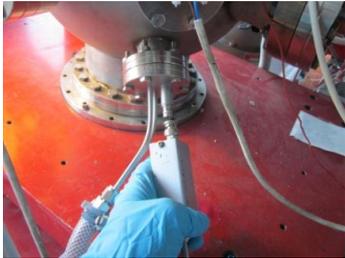
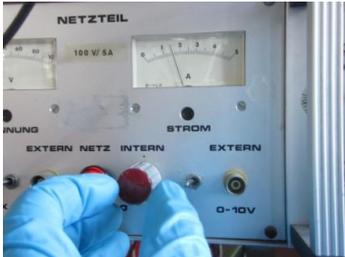
Appendix A: Recipe for p6P deposition

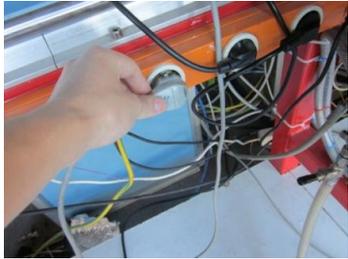
#	Process Description	Photos
1	<p>Initial conditions: The chamber is pumped down. The front valve between the turbo pump and the rough pump is open. The back inlet valve for the nitrogen is closed. The pressure in the chamber should be around 10-7mbar</p>	
2	<p>Turn off the fine pump of the transfer chamber</p>	
3	<p>Wait around 30mins until the turbine slow down, open and adjust the nitrogen pressure. Low pressure is needed</p>	
4	<p>Connect the nitrogen tube to the gas valve of the transfer chamber, and turn on the nitrogen valve</p>	
5	<p>Then turn on the gas valve of the transfer chamber slowly.</p>	
6	<p>When the sound of the turbine is fade away, and the table is moveable, then loose the screws</p>	

#	Process Description	Photos
7	Prepare the substrate. Remember to wear the gloves	
8	Use the tape to split the mica	
9	Fix the mica on the plate	
10	Choose the short screws to make sure there is not any tips come out of the plate	
11	Put the substrate into the transfer chamber with clamp.	
12	Rotate the transfer rod to fix the substrate on the rod	

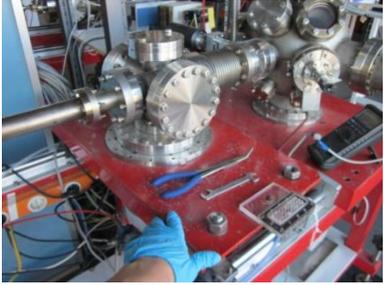
#	Process Description	Photos
13	Cover the transfer chamber, tight the screws	
14	Turn off the gas valve of the transfer chamber	
15	Turn off the nitrogen valve	
16	Close the valve of main chamber to seal off the main chamber from the rough pump	
17	Open the valve of the transfer chamber to rough pump the chamber	
18	Wait for a while(several minutes), when the pressure of the transfer chamber reached about 10^{-2} mbar, turn on the fine pump of the transfer chamber	

#	Process Description	Photos
19	Next, open the valve of the main chamber, connect the main chamber to the rough pump	
20	30mins~45mins later, the vacuum of transfer chamber reached almost the same vacuum of main chamber, open the air valve on the wall	
21	Insert the plug to open the pneumatic valve, which sealed off the transfer chamber from main chamber	
22	By using the transfer rod to fix the substrate on the holder in main chamber	
23	Extract out the plug to turn off the pneumatic valve	
24	Turn off the air valve on the wall	

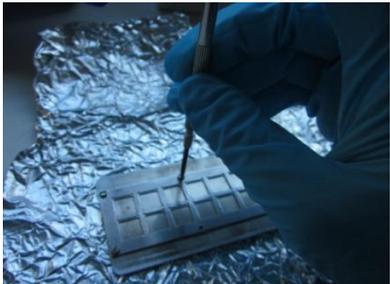
#	Process Description	Photos
25	Connect the microbalance	
26	Set temperature and turn on the thermo coax cables to heat the sample holder. (In our P6P deposition experiment, we set the holder temperature is around 480K)	
27	Turn on the thermo coax cables to warm the oven. Using the current to control the temperature. First, adjust the voltage to maximum, then adjust the current.	
28	Set the current at 1.6A at first to warm the oven, 2hours later, increase the current to 2.2A	
29	Around 20mins later, once the deposit rate keep stable at $0.1\text{\AA}/\text{s}$, clean off the data to remeasure the deposit data	
30	Open the shutter and start to deposit	

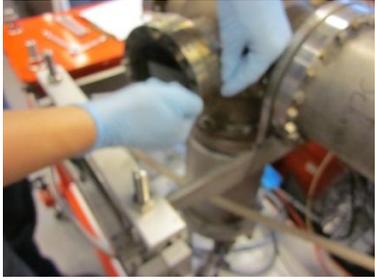
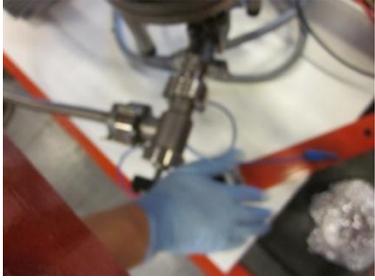
#	Process Description	Photos
31	Read and record the deposition data. In our P6P deposition experiment, $T_{\text{holder}}=207^{\circ}\text{C}$, $P=1.4 \times 10^{-8} \text{mbar}$, Rate= 0.1 \AA/s , Thickness= 5nm	
32	Once the thickness reached the designed value, close the shutter to stop the deposition. Turn off the heater of the oven, return the voltage and current to the minimum.	
33	Turn off the heater of the holder to cool down the sample.	
34	After 60mins, insert the plug of the pneumatic valve	
35	Turn on the air valve on the wall to open the pneumatic valve	
36	Insert the transfer rod into the main chamber	

#	Process Description	Photos
37	Fix the substrate on the transfer rod, then transfer it back to the transfer chamber	
38	Extract out the plug and turn off the air valve on the wall to close the pneumatic valve again	
39	Close the valve of the transfer chamber	
40	Turn off the fine pump of the transfer chamber	
41	Wait around 30mins until the turbine slow down, Connect the nitrogen tube to the gas valve of the transfer chamber, and turn on the nitrogen valve	
42	Next, turn on the gas valve of the transfer chamber slowly.	

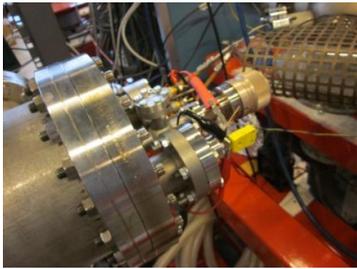
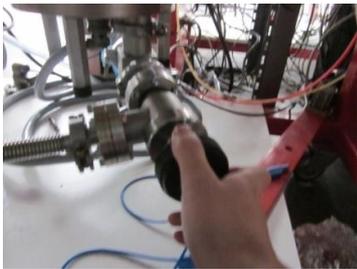
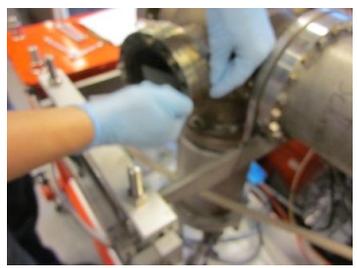
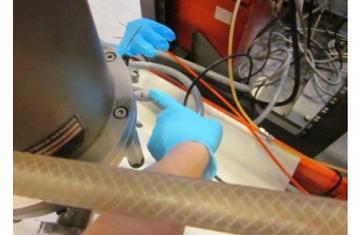
#	Process Description	Photos
43	When the sound of the turbine is fade away, and the table is moveable, then loose the screws of transfer chamber	
44	Open the chamber, get the substrate out	
45	Then close the transfer chamber and pump down it, just like what we did before. Finally, keep everything in the original state	
46	Put the deposited mica in the container and use the fluorescence microscope to inspect it	

Appendix B: Recipe for PPTTP deposition

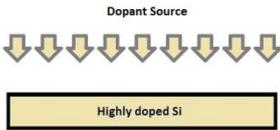
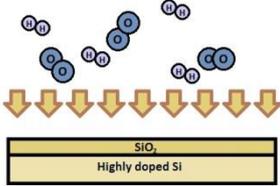
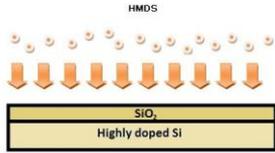
#	Process Description	Photos
1	<p>Initial conditions:</p> <p>The chamber is pumped down.</p> <p>The front valve between the turbo pump and the rough pump is open.</p> <p>The back inlet valve for the nitrogen is closed.</p> <p>The pressure in the chamber should be around 10^{-8}mbar</p>	
2	<p>Close the valve at the front, disconnecting the transfer chamber from the rough pump</p>	
3	<p>Turn off the turbo pump, by pressing stop on the power supply for the pump.</p> <p>Wait 20-30 min in order for the turbo pump to decrease in fan speed</p>	
4	<p>Loosen the nuts for the flange on the transfer chamber, but do not remove, in order to let nitrogen pass when pressurizing.</p>	
5	<p>Connected nitrogen and slowly open the inlet valve at the back (facing the chamber, turn the valve screw to your direction to open it). Fill the glove with nitrogen in small steps by watching the pressure detector. Turn off nitrogen and close inlet valve (when reach to 10^3mbar).</p>	
6	<p>Prepare the substrate and fix it on the holder and lock it with the grid.</p>	

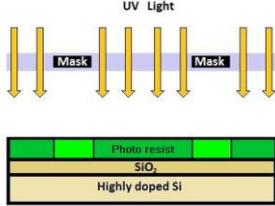
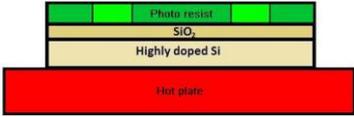
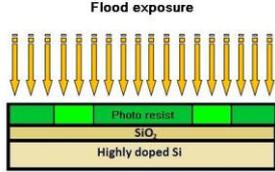
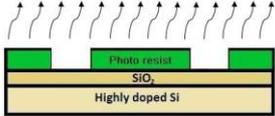
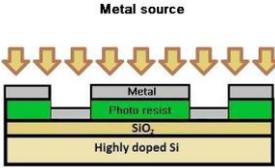
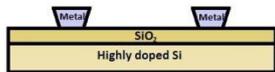
#	Process Description	Photos
7	Put the sample in the chamber and fasten with the two screws, be careful not to let them drop down into the turbo pump.	
8	Put the flange back on.	
9	Open the front valve for the rough pump. Reverse half circle.	
10	Wait a couple of minutes then start the turbo pump.	
11	The chamber now needs to pump down. This takes several hours and the above can therefore be carried out the day before. And set the temperature controller for the holder to around half of the desired temperature (For example 100°C).	
12	Turn on power supply for the holder and set current to around 2.07A. (Red light means current is constant, green light means voltage is constant. Only need to press "powder" and "output" buttons. "tracking" is used to control one heater working for another.)	

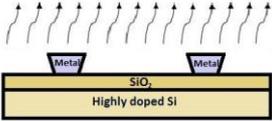
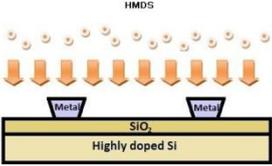
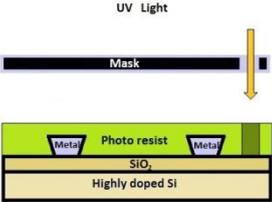
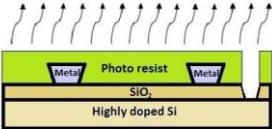
#	Process Description	Photos
13	Next day increase holder temperature to the desired temperature, like 160°C and oven current to 1,2A. (power supply: left side in charge of the holder, right side in charge of the oven)	
14	Leave the chamber for 3-4 hours in order for the temperature of the sample to be high enough	
15	When high enough turn oven current up to 2,0A. Measure the oven temperature by ampere meter. When the temperature reached around 390K, it is suitable for the deposition.	
16	Rotate the sample to be parallel with the deposition direction and turn on the shutter for the oven (mark 2). This way the deposition rate may be monitored before the actual deposition.	
17	Turn on the deposition detector (press "program" to choose crystal status 2). After about 40 min. there should be a deposition rate around 0,0-0,1 Å/sec. Press "zero" to clean the value to start the measurement.	
18	Turn sample to be perpendicular to the deposition direction and deposit around 4-6 nm. (When deposited at around 4nm, turn off the oven power, the deposition still goes on to 4-6 nm)	

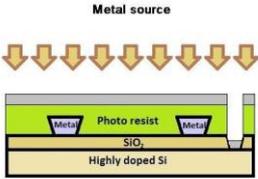
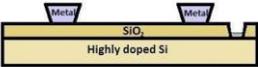
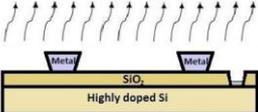
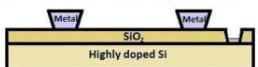
#	Process Description	Photos
19	Turn of the power supplies for the oven and the sample holder. Turn off the shutter (mark 0). Wait a while for the temperature of the sample holder to drop.(around 2~3hours)	
20	Start the process for ventilating the chamber: Close the valve at the front, disconnecting the transfer chamber from the rough pump.	
21	Turn of the turbo pump, by pressing stop on the power supply for the pump. Wait 20-30 min in order for the turbo pump to decrease in fan speed.	
22	Loosen the nuts for the flange on the transfer chamber, but do not remove, in order to let nitrogen pass when pressurizing.	
23	Connected nitrogen and slowly open the inlet valve at the back. The nitrogen may connect to another system. Fill the glove with nitrogen in small steps and open the valve in very small step. Turn of nitrogen and close inlet valve.	
24	Take out the sample. Then close the flange, turnoff the valve, use the rough pump to pump down for a while, next turn on the tube pump.	

Appendix C: Former Photolithograph Recipe of Transistor Substrate

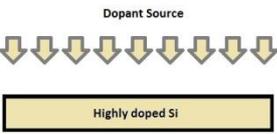
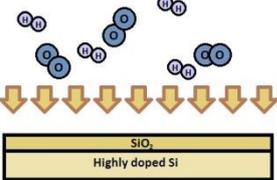
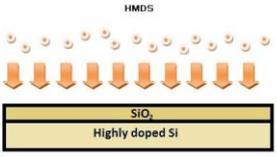
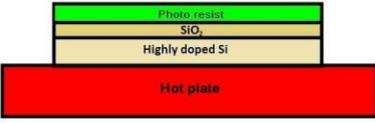
#	Process	Drawing	Description
1	Wafer cleaning		To keep the surface clean prepared for the next process
2	Doping and annealing		To form the gate which has low resistivity
3	Oxidation		To for the Silicon Dioxide layer, which will isolate the gate from the drain electrodes and the nanowire
4	1st Deposit adhesion promoter(HMDS)		To get a better photo resist application
5	Photo resist application		EBS11 spin coater, resist: AZ 5214E, resist thickness=1.5um Automatic resist dispense Spin at 500 rpm for 5s(acc. 5000 rps2) Spin at 4000 rpm for 30s(acc. 10000 rps2)
6	Prebake		Hot plate, 90oC for 60 s.

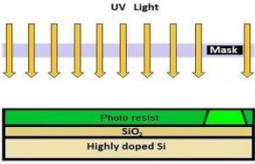
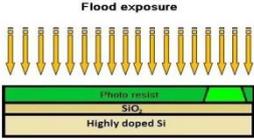
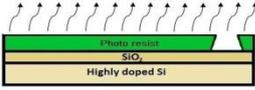
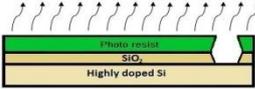
7	UV exposure		KS Mask aligner, exposure time = 2.1s
8	Inversion bake		Hot plate, 130oC for 100s
9	Flood exposure		Making the resists, which was not exposed in the 6th step, soluble in developer. Exposure time=25s, no mask.
10	Develop		Developer: AZ 351B (mix with DI water, ratio 1:4), agitation 1) 60s rough 2) 60s fine
11	1st Rinse and dry		Rinse in water(fine rinse bath) for 2 min, spin dry
12	1st Metal deposition		To form the saurce and drain electrodes Ti -10nm(to get a better Ag deposition) Ag-50nm
13	1st Resist removal		Got the saurce and drain electrodes Lift off metal by using the ultra-sonic clean-150s Rough clean-60s Fine clean-60s

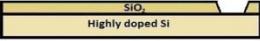
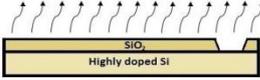
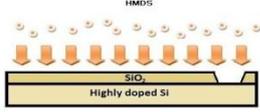
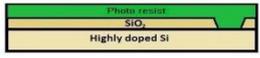
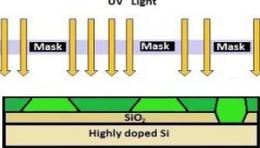
14	2nd Rinse and dry		Rinse in water(fine rinse bath) for 2 min, spin dry
15	2nd Deposit adhesion promoter(HMDS)		To get a better photo resist application
16	The 2nd photo resist application		Now a positive one
17	Exposure		To form a etch mask
18	Development		To form a way to the gate
19	Etching		As the thickness of SiO2 is 100 nm and RHF ≈ 75 nm/min So the etch time: 100s
20	3rd Rinse and dry		Remove HF: HF rough risen: 150s HF fine risen: 150s

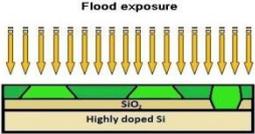
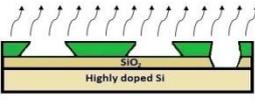
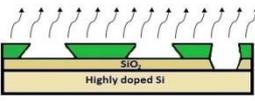
21	2nd Metal deposition		Cover the Si layer to prevent it oxidational Ti -10nm(to get a better Ag desposition) Ag-50nm
22	2nd Resist removal		Lift off metal by using the ultra-sonic clean-150s Rough clean-60s Fine clean-60s
23	4th Rinse and dry		Rinse in water(fine rinse bath) for 2 min, spin dry
24	Inspection		Check the work

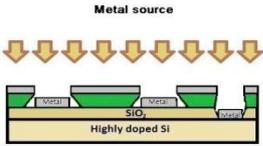
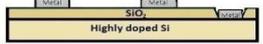
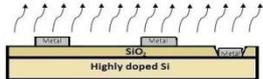
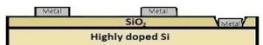
Appendix D: Improved Photolithograph Recipe of Transistor Substrate

#	Process	Drawing	Description
1	Wafer cleaning		Keep the surface clean prepared for the next process
2	Doping and annealing		Form the gate which has low resistivity
3	Oxidation		To form the Silicon Dioxide layer, which will isolate the gate from the drain electrodes and the nanowire
4	1 st Deposit adhesion promoter(HMDS)		To get a better photo resist application. Warm up the oven, and deposit HMDS under 120°C for 35mins. Then cool down for 10mins.
5	1 st Photo resist application		EBS11 spin coater, resist: AZ 5214E, resist thickness=1.5μm Automatic resist dispense:4s, no rotation Spin at 500 rpm for 5s(acc. 5000 rps ²) Spin at 4000 rpm for 30s(acc. 10000 rps ²)
6	1 st Prebake		Hot plate, 90°C for 60 s.

7	1 st UV exposure		KS Mask aligner, exposure time = 1.8s, 2.2s, 2.6s, 3.0s
8	1 st Inversion bake		Hot plate, 130°C for 100s
9	1 st Flood exposure		Making the resists, which was not exposed in the 7 th step, soluble in developer. Exposure time=30s, no mask.
10	1 st Develop		Developer: AZ 351B (mix with DI water, ratio 1:4), agitation, 60s under 22 °C
11	1 st Rinse and dry		Rinse in water 60s rough rinse 60s fine rinse Spin dry
12	Etching		To form a way to the gate. As the thickness of SiO ₂ is 100 nm and R _{HF} ≈75nm/min So the etch time:100s
13	2 nd Rinse and dry		Remove HF: 1) HF rough rinse 150s 2) HF fine rinse 150s 3) Spin dry

14	1 st Resist removal		Strip the resist in Acetone for around 4mins
15	3 rd Rinse and dry		Rinse in water 60s rough rinse 60s fine rinse Spin dry
16	2 nd Deposit adhesion promoter(HMDS)		To get a better photo resist application Prepare to form the source and drain electrodes
17	2 nd Photo resist application		EBS11 spin coater, resist: AZ 5214E, resist thickness=1.5μm Automatic resist dispense:4s, no rotation Spin at 500 rpm for 5s(acc. 5000 rps ²) Spin at 4000 rpm for 30s(acc. 10000 rps ²)
18	2 nd Prebake		Hot plate, 90°C for 60 s
19	2 nd UV exposure		KS Mask aligner, exposure time = 1.8s, 2.2s, 2.6s, 3.0s

20	2 nd Inversion bake		Hot plate, 130°C for 100s
21	2 nd Flood exposure		Exposure time=25s, no mask
22	2 nd Develop		Developer: AZ 351B (mix with DI water, ratio 1:4), agitation 60s under 22 °C
23	4 th Rinse and dry		Rinse in water 60s rough rinse 60s fine rinse Spin dry
24	Dip in HF		To get a better contact with metal electrodes Dip in HF for 10s
25	5 th Rinse and dry		Remove HF: HF rough risen:150s HF fine risen: 150s Spin dry

26	Metal deposition	 <p>The diagram shows a cross-section of a substrate labeled 'Highly doped Si'. A thin layer of 'SiO₂' is on top. There are three rectangular regions of 'Metal' on the surface. Above these regions, seven downward-pointing arrows are labeled 'Metal source', indicating the direction of metal deposition.</p>	<p>To form the source and drain electrodes Ti -10nm(to get a better Au desposition) Au-50nm</p>
27	2 nd Resist removal	 <p>The diagram shows the substrate after the second resist removal. The 'Metal' regions are now clearly visible on the 'SiO₂' layer, and the resist has been removed from the non-metal areas.</p>	<p>Lift off metal and resist by using the ultra-sonic clean in Acetone for 4 mins</p>
28	6 th Rinse and dry	 <p>The diagram shows the substrate after the sixth rinse and dry. The 'Metal' regions are now fully defined on the 'SiO₂' layer. Above the metal regions, several upward-pointing arrows indicate the direction of the rinse water.</p>	<p>Rinse in water 60s rough rinse 60s fine rinse Spin dry</p>
29	Inspection	 <p>The diagram shows the final inspection stage. The 'Metal' regions are clearly visible on the 'SiO₂' layer, and the substrate is labeled 'Highly doped Si'.</p>	<p>Check the work</p>

Appendix E: Recipe of Dicing

#	Process Description	Image
1	Connect the valve at right on the wall	
2	Mount the spindle at left. Be careful about the water pipe on the spindle.	
3	Mount the protective windows	
4	Turn on the equipment in power supply under equipment, then turn on the red valve.	
5	Press the <i>power</i> button in the keyboard	

6	Check if the air is ok in the panel. Then adjust the speed under equipment(around 20)	
7	Set the parameters: <i>Index1</i> : distance between 2 lines in X-axis <i>Index2</i> : distance between 2 lines in Y-axis(useless as we choose semi-auto mode) <i>Size</i> : the size of the wafer(100mm) <i>Height</i> : the height to be left after cutting(0.15mm) Select the parameter, press the "GO"	
8	Turn on the <i>illumination</i> (2lights)	
9	Turn on the <i>spindle</i>	
10	Press the button " <i>set up</i> " once. This will measure the plate height	
11	Mount the wafer more or less in the centre of plate	
12	Press <i>vacuum</i> . Check in the vacuum in the panel(should be in green area)	

13	Adjust the region to be cut. It must fit the lowest horizontal line in the screen	
14	Adjust the wafer position with sets in keyboard. Drive modes: <i>scan</i> -final adjustments <i>Index</i> -move in the step adjusted in index1	
15	Rotate the wafer until it is aligned in the screen	
16	When is everything sat, press " <i>semi-auto</i> ". Then, the water starts to flow. Press " <i>front</i> ↓" or " <i>rear</i> ↑", so the cutting process starts.	
17	When is finished, press " <i>semi-auto</i> " again.	
18	Press " <i>index1</i> " and select the step for Y-axis. Rotate the wafer in 90°. Align the wafer again	
19	Repeat the cutting process	
20	After the process is finished, turn off the illumination, vacuum and spindle	
21	Take out the protective window	
22	Blow the water, from up to down.	
23	Take out the wafer, then take out the spindle and dry the equipment	
24	Turn off the red valve and the power supply. Turn off the valve at wall (it use to pump the particle or dust during the dicing. It will make the noise)	

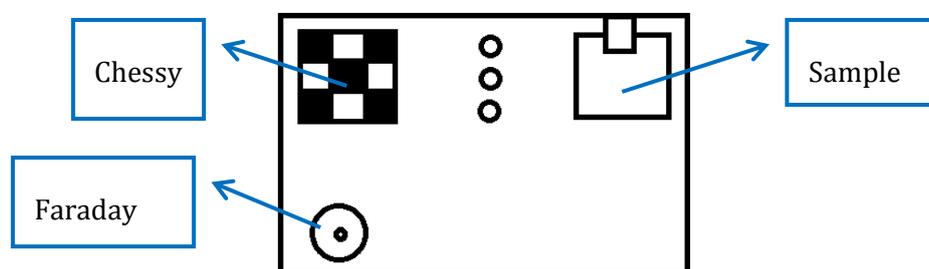
Appendix F: Step by Step Procedure of EBL

Equipment:

HITACHI model S-4800 field emission SEM

Process:

1. Resist application: PMMA A4 (the concentration of PMMA) 200nm spin coating (program 4): a) 1500rpm 5s. b) 7000 rpm 4.5s
2. Bake 200°C for 90s
3. Sample holder: lock the sample on the holder. (Remember to mark the cross signs, in order to find them easily under SEM)



4. Pump down the chamber: AIR(vent)/EVAC(pump down)
5. Open the chamber, transfer sample and close chamber.
6. Press " Home" on computer operation window to send the sample holder insider.
7. Adjust the current: move lens to Faraday cap, set the parameters: 2.00k, 30KV, 1.1μA. Open the current measurement device and choose range in 200PA. Keep certain distance from the device in order to reduce the background noise. Usual value of the current should be around 11.2PA(0.0112nA), the range from 0.018 to 0.02nA is ok.
8. In exposure window of computer, exposure calculation, input the beam current just measured before.
9. Dwell time calculation: including line and dot dwell time
10. Chessy Pattern Alignment: move lens to chessy pattern, H/L set to 400x, then set to 10.0Kx, press " align".
Beam align: use X, Y alignment to adjust the white spot to the center
Stigma align X/Y: use X, Y alignment to stable the image
Set to 500x, find the center of the square, choose Microscope control, choose SET, click right button to choose 500x, 100.0μm.
Right click button to choose SET, open new position list, open scan manager, Align write field procedures, choose 100μm WF, drag it into the position list window, press F9 (or scan selection), press "ctrl" and drag the square image in to the center, continue to adjust 4 square.
Close position list, without save it.
11. Sample Alignment: press" Beam off/on" to choose "on" and "internal", move lens back to sample, find the cross mark.

Set 900x, RED I to focus the view. Set back to 500x to find the left cross mark into the centre of the view.

Press “adjustment”, “origin correction”, “adjust”.

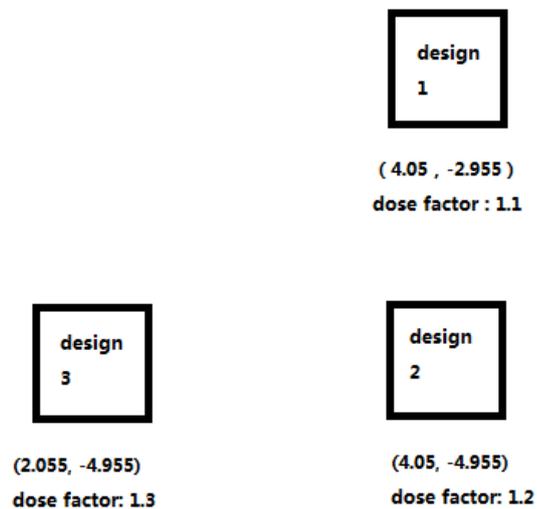
In Angle Correction, in label 1 press “accepted” button. In “stage control”, “drive”, “U” blank, input 6mm, press “start”, lens move to the right cross mark.(U:X, V:Y)

Find the right cross mark, in Label 2 press “accepted” button, press “adjust”, then go back to the left cross mark or the original point.

Set 500x, in microscope control, set 500x, 100µm, right click button “SET”

12. Open the position list, press “design”, find the design files(for example: light emission_new.gds), open the file. Drag the design file into position list, right click “properties”, click “select exposed layer”, choose “All”, press “ok”.

In exposure properties, input the design images coordinates and dose factor (test several dose factors then choose the best one).



13. In position list, choose all ID, make sure “Beam off”, press “scan selection”, and magnification is 500x.
14. When the lights in position list are all bright, means scanning finished. Press “Home” to send the sample to the original place, press “EXC” to send the sample out. Then take it out of the chamber.
15. Developing: 45s in Developer(MIBK:IPA=1:3), 30s in stopper(IPA)
Fill the log of EBL: sample is smaller than 5µmX5µm just mark one “cross”, larger than that, mark two “cross”
Put the waste liquid in organic C
16. Metal deposition
17. Put sample in Remover PG at least 2 hours to strip off
18. Water, rinse and dry

Appendix G: Program to Measure the light intensity in Voltage

Sweeping Test

The program is made by Per Baunegaard With Jensen, with a little charges to suit for the measurements in this project.

```
clear all
close all
clc

%% Constants
TF=31; %Size of the target area of the image
APM=9; %Size of the matrix around the peak
for average. Should be uneven.

%% Start
pic=imread('sweeping V\3.4V250kHz.tif'); %Path for image with
maxium voltage. Set manually
imagesc(pic); title('Left click mouse to select spots. Press enter to
continue.')
```

```
[x,y]=ginput %Graphical input for one or several
peak position
figure;
MAX=length(x); %Number of x (and y) values. Used for
loop boundary
SRT=double(int32(sqrt(MAX)))+1; %Variable for subplot dimensions
for l=1:1:MAX; %Looped to proces multiple peaks
if x(l)-(TF/2)<0 %If the input position lies to
close to the edge it is detected here
TF=x(l); %The target area is reduced to fit
inside the image
elseif x(l)+(TF/2)>1000
TF=1000-x(l);
elseif y(l)-(TF/2)<0 %The same for y
TF=y(l);
elseif y(l)+(TF/2)>1000
TF=1000-y(l);
end
TF=int32(TF);
TF=double(TF); %The target area variable is made
integer and then double because of later use.
```

```

xclip(:,1)=(int32(x(1))-TF/2:int32(x(1))+TF/2);    %xclip is an array
for the x values of the target area centeret at the input x value
yclip(:,1)=(int32(y(1))-TF/2:int32(y(1))+TF/2);    %yclip is an array
for the y values of the target area centeret at the input y value
xclip(:,1)=double(xclip(:,1));                    %converted to double
variable because of future process
yclip(:,1)=double(yclip(:,1));
ext=pic(yclip(:,1),xclip(:,1));                    %ext now contains all
values in the target area
Points{1}=sprintf('Point %d',1);                  %Legend for number of selected
points
subplot(SRT,SRT,1);imshow(ext)                    %and is plotted to show if the
peak is inside the target area
title(Points{1});                                  %use points legend for title of
each selected peak
end
figure;
imagesc(pic);                                     %Plot image with selected
peaks/points
hold on;
plot(x,y,'or','linewidth',5);
text(x+25,y,cellstr(Points),'Color','r');
hold off;

%% Voltage vs intensity analysis
V=[1:0.2:3.4];                                     %Array of measured Voltages. Set manually
for l=1:1:MAX;                                     %Looped to proces multiple peaks
    %figure;
for k=1:1:length(V);

pic=imread(sprintf('sweeping V/%.1fV250kHz.tif', V(k))); %load image.
Set path manually
ext=pic(yclip(:,1),xclip(:,1));                    %procure
the target area from the image
L(k,1)=double(max(max(ext)));                       %fin
d the maximum values in the target area
[U,J]=find(ext==L(k,1));                             %find the
(x,y) values of those values
MU=int32(mean(U));                                   %in case of
several maximum values
MJ=int32(mean(J));                                   %an average of
the (x,y) are taken

```

```

APVM=pic((yclip(1,1)+MU-(double(int32(APM/2))):yclip(1,1)+MU+(double(
int32(APM/2)-2))), (xclip(1,1)+MJ-(double(int32(APM/2))):xclip(1,1)+MJ
+(double(int32(APM/2)-2))));
%APVM                                     %Average peak
value matrix is found above and contains the values for averaging the peak
value. Centeret around the average of (x,y) for the maximum values
Lid(k,1)=mean2(APVM);                                     %the
average of the average peak value matrix
%subplot(6,5,k);
%imagesc(ext);
%hold on;
%plot(MJ,MU,'kx','linewidth',10); %Plots of the target area for all
images with a X to mark the average peak centrum
%title(sprintf('%0.0fV 250kHz.tif', V(k)*25))
%hold off;
end
end
figure;
plot(V*25,L,'-*');xlabel('Gate voltage amplitude
(V)');ylabel('Electroluminescence intensity (a.u.)');title('Max peak
value, f_0=250kHz');
legend(Points{:});
figure;
plot(V*25,Lid,'-x');xlabel('Gate voltage amplitude
(V)');ylabel('Electroluminescence intensity (a.u.)');title('Average
peak value, f_0=250kHz');
legend(Points{:});
%Plot of the maximum and the averaged peak values as a function of
%voltage
W=mean(L');
Wid=mean(Lid');
H=std(L');
Hid=std(Lid');

if MAX>1 %only execute if there is multiple points
figure;
subplot(1,2,1);errorbar(V*25,W,H);xlabel('Gate voltage amplitude
(V)');ylabel('Electroluminescence intensity
(a.u.)');title('f_0=250kHz');
legend('Average from all points max peak value');
subplot(1,2,2);errorbar(V*25,Wid,Hid);xlabel('Gate voltage amplitude
(V)');ylabel('Electroluminescence intensity
(a.u.)');title('f_0=250kHz');
legend('Average from all points average peak value');

```

```
figure;
semilogy(V*25,W,'-*',V*25,Wid,'-x');xlabel('Gate voltage amplitude
(V)');ylabel('Electroluminescence intensity
(a.u.)');title('f_0=250kHz');
legend('Average from all points max peak value','Average from all points
average peak value');
%Plot of the averaged over multiple points of the above as a function of
%voltage
else
end

%% Exporting data
Ud2=[(V*25) ' W' H' Wid' Hid'];
save(['FET22_Voltage_' num2str(length(Points)) '_points.txt'], 'Ud2',
'-ascii', '-tabs');
```

Appendix H: Program to Measure the light intensity in Frequency

Sweeping Test

The program is made by Per Baunegaard With Jensen, with a little charges to suit for the measurements in this project.

```
clear all
close all
clc

%% Constants
TF=31; %Size of the target area of the image
APM=9; %Size of the matrix around the peak
for average. Should be uneven.

%% Start
pic=imread('Frequency\up\60kHz1V.tif'); %Path for image with
maxium voltage. Set manually
imagesc(pic); title('Left click mouse to select spots. Press enter to
continue.')
```

```
[x,y]=ginput %Graphical input for one or several
peak position
figure;
MAX=length(x); %Number of x (and y) values. Used for
loop boundary
SRT=double(int32(sqrt(MAX)))+1; %Variable for subplot dimensions
for l=1:1:MAX; %Looped to proces multiple peaks
if x(l)-(TF/2)<0 %If the input position lies to
close to the edge it is detected here
TF=x(l); %The target area is reduced to fit
inside the image
elseif x(l)+(TF/2)>1000
TF=1000-x(l);
elseif y(l)-(TF/2)<0 %The same for y
TF=y(l);
elseif y(l)+(TF/2)>1000
TF=1000-y(l);
end
TF=int32(TF);
TF=double(TF); %The target area variable is made
integer and then double because of later use.
```

```

xclip(:,1)=(int32(x(1))-TF/2:int32(x(1))+TF/2);    %xclip is an array
for the x values of the target area centeret at the input x value
yclip(:,1)=(int32(y(1))-TF/2:int32(y(1))+TF/2);    %yclip is an array
for the y values of the target area centeret at the input y value
xclip(:,1)=double(xclip(:,1));                    %converted to double
variable because of future process
yclip(:,1)=double(yclip(:,1));
ext=pic(yclip(:,1),xclip(:,1));                    %ext now contains all
values in the target area
Points{1}=sprintf('Point %d',1);                  %Legend for number of selected
points
subplot(SRT,SRT,1);imshow(ext)                    %and is plotted to show if the
peak is inside the target area
title(Points{1});                                  %use points legend for title of
each selected peak
end
figure;
imagesc(pic);                                      %Plot image with selected
peaks/points
hold on;
plot(x,y,'or','linewidth',5);
text(x+25,y,cellstr(Points),'Color','r');
hold off;

%% Frequency vs intensity analysis
Hz=[10:5:60];                                     %Array of measured frequencies. Set manually
for l=1:1:MAX;                                     %Looped to proces multiple peaks
    %figure;
    for k=1:1:length(Hz);

pic=imread(sprintf('frequency/up/%dkHz1V.tif', Hz(k))); %load image.
Set path manually
ext=pic(yclip(:,1),xclip(:,1));                    %p
rocure the target area from the image
M(k,1)=double(max(max(ext)));                       %f
ind the maximum values in the target area
[U,V]=find(ext==M(k,1));                            %find the
(x,y) values of those values
MU=int32(mean(U));                                  %in case of
several maximum values
MV=int32(mean(V));                                  %an average of
the (x,y) are taken
APVM=pic((yclip(1,1)+MU-(double(int32(APM/2))):yclip(1,1)+MU+(double(
int32(APM/2))-2)),(xclip(1,1)+MV-(double(int32(APM/2))):xclip(1,1)+MV

```

```

+ (double(int32 (APM/2)) - 2));
%APVM %Average peak
value matrix is found above and contains the values for averaging the peak
value. Centeret around the average of (x,y) for the maximum values
Mid(k,1)=mean2 (APVM); %the
average of the average peak value matrix
%subplot(7,6,k);
%imagesc(ext);
%hold on;
%plot(MV,MU,'kx','linewidth',10);
%title(sprintf('%.1fkHz 3.0V', Hz(k))); %Plots of the target area for
all images with a circle to mark the average peak centrum
%hold off;
end
end
figure;
plot(Hz,M,'-*');xlabel('Frequency (kHz)');ylabel('Electroluminescence
intensity (a.u.)'); title('Max peak value, Gatevoltage 25V');
legend(Points{:});
figure;
plot(Hz,Mid,'-x');xlabel('Frequency
(kHz)');ylabel('Electroluminescence intensity (a.u.)'); title('Average
peak value, Gatevoltage 25V');
legend(Points{:});
%Plot of the maximum and the averaged peak values as a function of
%frequency
Q=mean(M');
Qid=mean(Mid');
S=std(M');
Sid=std(Mid');

if MAX>1 %only execute if there is multiple points
figure;
subplot(1,2,1);errorbar(Hz,Q,S);xlabel('Frequency
(kHz)');ylabel('Electroluminescence intensity (a.u.)');
title('Gatevoltage 25V');
legend('Average from all points max peak value');
subplot(1,2,2);errorbar(Hz,Qid,Sid);xlabel('Frequency
(kHz)');ylabel('Electroluminescence intensity (a.u.)');
title('Gatevoltage 25V');
legend('Average from all points average peak value');
figure;
semilogy(Hz,mean(M),'-*',Hz,mean(Mid),'-x');xlabel('Frequency
(kHz)');ylabel('Electroluminescence intensity (a.u.)');

```

```
title('Gatevoltage 25V');
legend('Average from all points max peak value','Average from all points
average peak value');
%Plot of the averaged over multiple points of the above as a function of
%frequency
else
end

%% Exporting data
Ud1=[Hz' Q' S' Qid' Sid'];
save(['FET22_Frequency_' num2str(length(Points)) '_points.txt'], 'Ud1',
'-ascii', '-tabs');
```

Appendix I: Short Circuit Test for Fabricated Electrodes of Transistors

Short circuit tests are carried out through probe station. It consists of a Stanford Research SR570 current pre-amplifier, a 16-bit National Instruments DAQ card, two Falco system DC voltage amplifier and three probers. The schematic diagram of the experimental setup is illustrated in fig. I.1

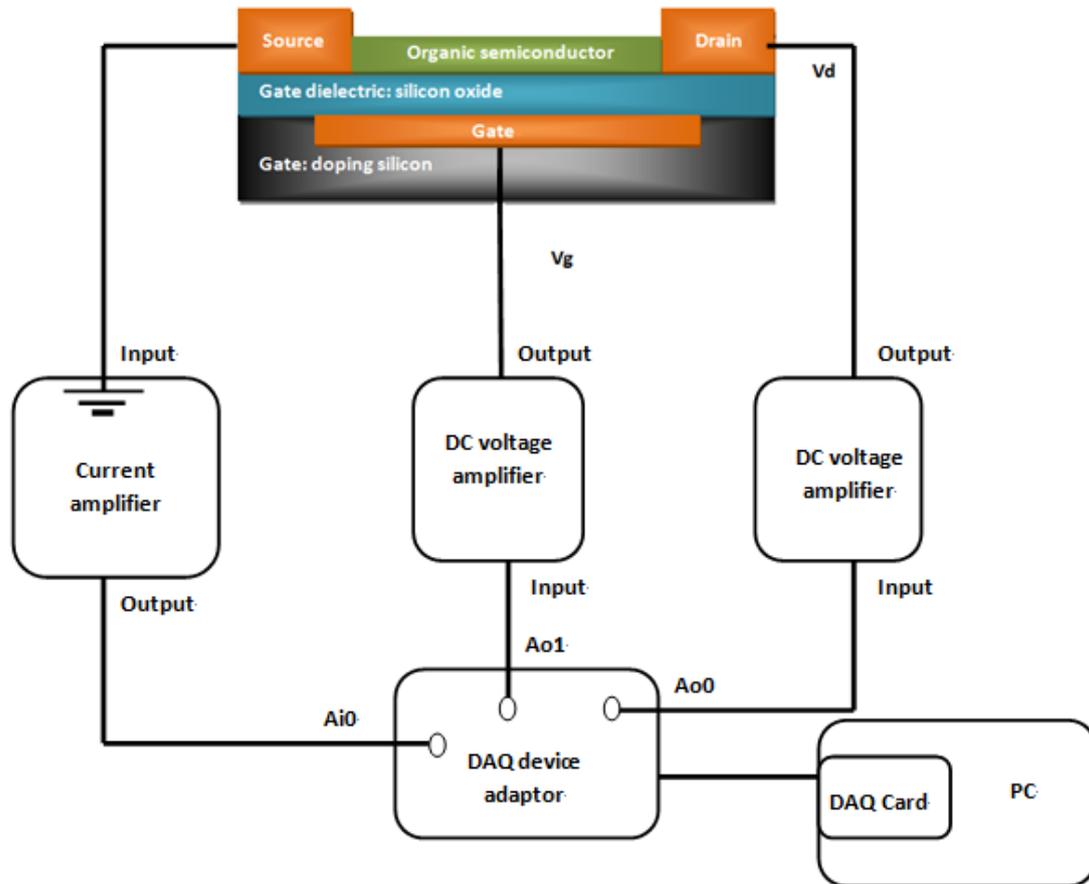


Fig.I.1: schematic diagram of probe station system

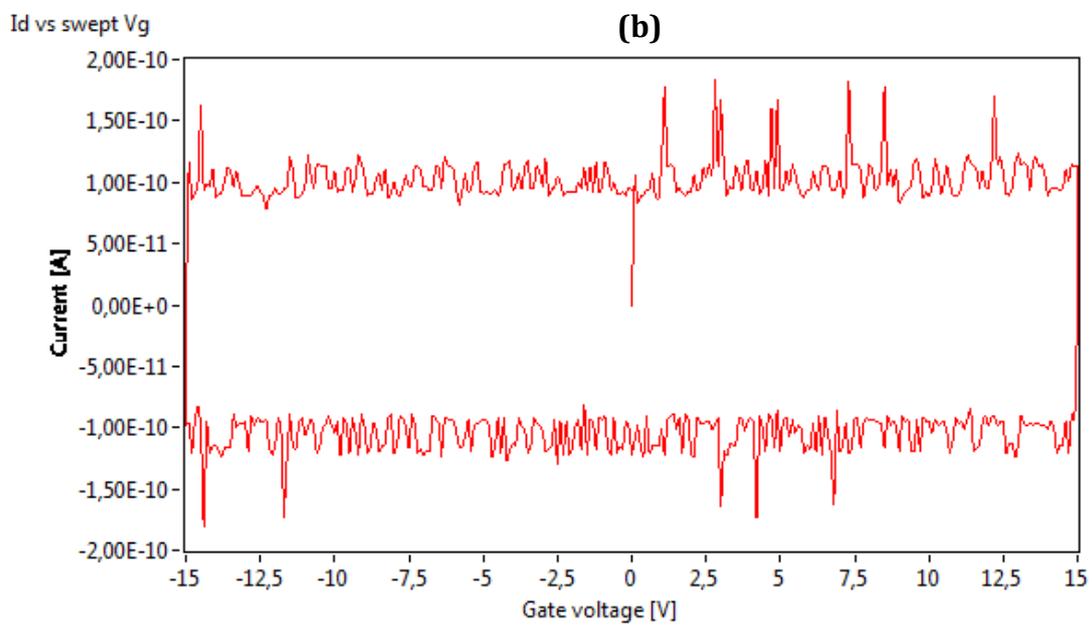
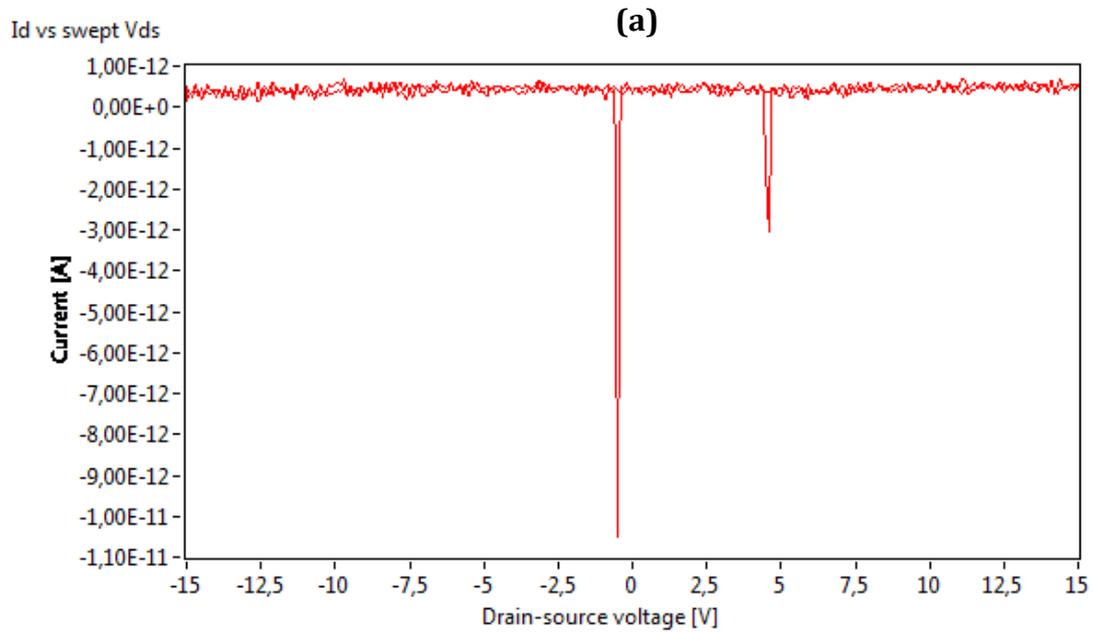
Three electrodes on the chip are connected to this circuit by three probers. The source is connected with the input end of SR570 current amplifier, which is grounded; while gate and drain are connected to DC voltage amplifiers with multiplier factor 20. The voltage signers are sent by DAQ card through DAQ device adaptor. As DAQ card can only provide a voltage up to 10 volt,so the DC voltage amplifiers are required.

For a good transistor substrate, there is not short circuit between drain and source. So when sweeping drain voltage V_d , the current I_d should float around zero (shown in fig.I.2 (a)).

Meanwhile, the current leak through the gate dielectric layer is not allowed. In this way, when sweeping the gate voltage V_g , for instance, from 0 to 15V, then decrease to -15V

and finally return to 0V, the dielectric layer should work as a capacitor, and current curve should form a “square” curves according to the sweeping V_g (shown in fig.I.2(b)).

Whereas, if there is a current leakage through the dielectric layer, then it will work as a resistance, as the current will increase according to the increasing V_g (shown in fig.I.2(c)).



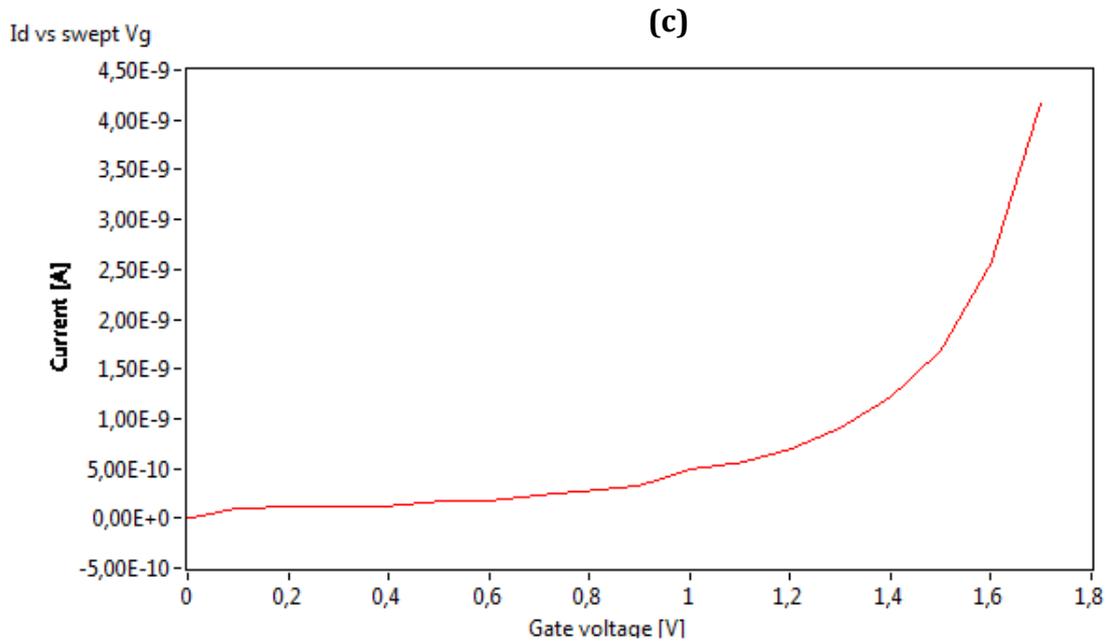


Fig.1.2: feature curves of the electrical test: a) sweeping the drain voltage, there is no short circuits between drain and source; b) sweeping the gate voltage, there is not current leakage; c) sweeping the gate voltage, the dielectric layer break down.

During the project, when I tested the chips fabricated by N3 wafer, the current leakage appeared as the dielectric layer is only 100nm thick, which might became thinner during the procedure of fabrication. So once a relative high gate voltage was applied, the insulator lay was very easy to breakdown and form the current leakage. As for the chips fabricated by N4 wafer, in which the SiO₂ is 200nm thick, they can support relative high gate voltage.

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